Exhibit D
Part 1

1	UNITED STATES PATENT AND TRADEMARK OFFICE
2	BEFORE THE PATENT TRIAL AND APPEAL BOARD
3	
4	
5	EMC CORPORATION,
6	Petitioner,
7	V.
8	ACQIS LLC,
9	Patent Owner.
LO	
L1	
L2	Case IPR2014-01462 (Patent 8,041,873 B2)
L3	Case IPR2014-01469 (Patent RE42,814 E)
L 4	
L 5	Thursday, August 27, 2015
L 6	
L7	Volume I of II
L 8	
L 9	Deposition of VOLKER LINDENSTRUTH, taken at the
20	offices of Gibson, Dunn & Crutcher, Carmelite House, 50
21	Victoria Embankment, London EC4Y ODZ, beginning at
22	8:57 a.m. before Audrey Shirley, QRR, ACR, MBIVR.
23	
24	
>5	

1	APPEARANCES
2	
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21	
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23	
24	
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1	I N D E X	
2		
3	Witness Examination	Page
4	Volker Lindenstruth (By Mr. Buroker)	4
5		
6		
7	EXHIBITS	
8		
9	Exhibit No. Description	Page
10	No. 1027 Document entitled "SCI	99
11	implementation study for LHCb Data Acquisition."	
12		
13		
14		
15		
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23		
24		
25		

1	VOLKER LINDENSTRUTH, having been duly sworn, was	
2	examined and testified as follows:	
3		08:57:36
4	MR. BUROKER: For the record we should	08:57:36
5	probably announce ourselves. My name is Brian	08:57:38
6	Buroker from Gibson, Dunn & Crutcher, I represent	08:57:41
7	the petitioner in both proceedings, EMC.	08:57:42
8	MR. DAVIS: My name is Britton Davis,	08:57:47
9	I'm with Cooley LLP, I represent the patentholder	08:57:48
10	in both proceedings.	08:57:54
11	THE WITNESS: I am Volker Lindenstruth,	08:57:56
12	I am the witness.	08:57:58
13	EXAMINATION	08:58:00
14	BY MR. BUROKER:	08:58:00
15	Q. For the record, Dr. Lindenstruth,	08:58:00
16	would you please state your full name?	08:58:03
17	A. Professor Dr. Volker Lindenstruth,	08:58:05
18	born in Frankfurt 1962, October 8th.	08:58:07
19	Q. And please state your full	08:58:15
20	business address?	08:58:16
21	A. I have several business addresses.	08:58:23
22	The primary office is in Frankfurt, it is	08:58:26
23	Ruth-Moufang Street. "Ruth" as "Ruth" dash	08:58:31
24	M-o-u-f-a-n-g Street No. 1 in Frankfurt. The zip	08:58:40
25	code I don't remember off the top of my head. If	08:58:43

1	you want me to dig it out.	08:58:47
2	Q. I don't think that's necessary.	08:58:48
3	A. Second address would be GSI	08:58:51
4	Helmholtz Center in Darmstadt, Helmholtz with	08:58:54
5	T-Z, Planck Street 1, like Max Planck, zip code	08:59:02
6	again don't remember.	08:59:07
7	Q. And then for the record if you	08:59:08
8	would please state your home address?	08:59:10
9	A. This is Hoch Strasse, H-o-c-h	08:59:13
10	Strasse German word for street 84, 55128,	08:59:28
11	Mainz, M-a-i-n-z.	08:59:40
12	Q. And just so we're clear, this	08:59:41
13	deposition is being taken pursuant to two U.S.	08:59:46
14	Patent and Trademark Office proceedings related	08:59:50
15	to Inter Partes Review 2014-01469 and	08:59:57
16	IPR2014-01462. Is that your understanding,	09:00:07
17	Dr. Lindenstruth?	09:00:12
18	A. I believe so, I have the two here.	09:00:13
19	I don't remember the numbers off the top of my	09:00:16
20	head. One is the '873, 8,041,873 and the other	09:00:19
21	is the US RE42814.	09:00:23
22	Q. Right, those are the patent	09:00:34
23	numbers. If you look also on those documents	09:00:35
24	there's an IPR number and what I called out was	09:00:37
25	for the '814 Patent the IPR proceedings is	09:00:41

1	IPR2014-01469; is that correct?	09:00:45
2	A. Yeah.	09:00:49
3	Q. And for the '873 Patent, the IPR	09:00:49
4	proceeding is IPR2014 01462; is that correct?	09:00:53
5	A. Okay, I didn't remember them	09:00:57
6	therefore I just checked.	09:00:59
7	Q. And you understand that your	09:01:00
8	testimony, although given here in the United	09:01:03
9	Kingdom, is as if you were giving testimony in	09:01:06
10	the United States, correct?	09:01:08
11	A. That's correct, yeah.	09:01:09
12	Q. And so that your testimony is	09:01:11
13	subject to penalty of perjury under the United	09:01:15
14	States law. Is that your understanding?	09:01:18
15	A. I understand that.	09:01:19
16	Q. Have you been deposed before?	09:01:20
17	A. In this kind of context, no.	09:01:23
18	Q. Is there another kind of context	09:01:25
19	in which you have been deposed?	09:01:27
20	A. I have been involved in several	09:01:29
21	cases of IP law where laws about compliance with	09:01:31
22	certain products and so forth, but never in such	09:01:39
23	a case, with a cross-examination.	09:01:43
24	Q. Were any of those cases related to	09:01:45
25	court proceedings in the United States?	09:01:49

1	A. No.	09:01:51
2	Q. Were those cases involving court	09:01:51
3	proceedings in Germany?	09:01:54
4	A. Leading to, yeah. But	09:01:57
5	Q. What do you mean well, were you	09:02:01
6	finished? I'm sorry.	09:02:04
7	Well, let me step back a minute. Since	09:02:04
8	you haven't been involved in a deposition, I'm	09:02:07
9	sure your counsel went over this with you but let	09:02:10
10	me explain the process and so forth. I'll ask	09:02:13
11	a question and if you don't understand my	09:02:16
12	question please let me know that you didn't	09:02:18
13	understand it so I can clarify, is that fair?	09:02:21
14	A. Sure.	09:02:23
15	Q. If you don't say anything I'm	09:02:24
16	going to assume you understood my question. The	09:02:27
17	second thing is because this court reporter is	09:02:30
18	doing a very good job and trying to keep track of	09:02:32
19	the questions and answers, it's important that	09:02:34
20	you wait for me to finish and I'll wait for you	09:02:36
21	to finish your answer and I apologize I may have	09:02:38
22	interrupted your last answer. So if you we can	09:02:41
23	try to do that it will make everything easier on	09:02:44
24	everybody involved, okay.	09:02:48
25	Is there any reason why you can't give	09:02:49

1	truthful testimony here today?	09:02:52
2	A. I'm not aware of any.	09:02:53
3	Q. No medications or anything that	09:02:54
4	you may be taking that would impair your ability	09:02:56
5	to testify truthfully?	09:02:58
6	A. No.	09:03:00
7	Q. Okay. So going back, what is the	09:03:00
8	nature of the proceedings in which you have given	09:03:07
9	testimony in the past?	09:03:10
10	A. Most cases are in the context of,	09:03:13
11	for example, we are spending a lot of money	09:03:18
12	buying computers, you have the public tender, you	09:03:24
13	set forth documents, what the product has to	09:03:29
14	comply with, product not being delivered and not	09:03:31
15	being delivered according to spec and then you	09:03:35
16	get into a fight with a vendor and normally it's	09:03:37
17	being resolved, sometimes not, and then you	09:03:41
18	prepare your way to the court. That's one	09:03:45
19	example.	09:03:47
20	Another example, product being delivered	09:03:48
21	and then turns out that there is a patent by	09:03:50
22	another vendor which prevents this product from	09:03:54
23	being used which of course is not a funny thing	09:03:57
24	to be once you've paid the product already, and	09:03:59
25	we're talking usually minimum €100,000 and more.	09:04:03

1	And then you prepare the case.	09:04:08
2	In most cases we could avoid going all	09:04:12
3	the way and settled one or the other way but, of	09:04:16
4	course, in order to get such a case without you	09:04:20
5	have to prepare it as if it was to go to court.	09:04:25
6	Q. So, breaking that down a little	09:04:30
7	bit, you have been involved in cases in which	09:04:34
8	companies or businesses you've been involved with	09:04:37
9	were accused of patent infringement; is that	09:04:40
10	correct?	09:04:43
11	A. In this one case there was no	09:04:45
12	direct infringement case yet raised, but I had	09:04:50
13	purchased a product for close to €200,000 where	09:04:53
14	subsequently the patent was issued in Germany	09:04:58
15	which prevented us to use that product. Since we	09:05:02
16	are public sector we can't just ignore the	09:05:05
17	existence of a patent and wait for the injunction	09:05:08
18	by the patent owner to stop us, right? I mean we	09:05:11
19	have high standards being the government. So	09:05:15
20	that had to be resolved.	09:05:18
21	Q. And in that proceeding did you	09:05:20
22	give testimony in court?	09:05:22
23	A. It didn't get that far	09:05:23
24	fortunately	09:05:25
25	Q. Have you	09:05:26

1	A that case.	09:05:26
2	Q. Oh sorry. Have you given	09:05:28
3	testimony in court proceedings anywhere in the	09:05:29
4	world before?	09:05:34
5	A. Once in Germany that was a suit	09:05:35
6	introduced by the University of Heidelberg	09:05:39
7	against somebody who basically copied an entire	09:05:43
8	class I did into a book under his own name, which	09:05:47
9	obviously was not a good thing to happen, in	09:05:51
10	particular because then later I had students	09:05:53
11	argue that I plagiarized the authors of that	09:05:57
12	particular book. That was the moment when I said	09:06:02
13	that had to stop. The publishing house refused	09:06:04
14	to do any remedy, so it went to court, the full	09:06:09
15	proceeding. And since this is a the judge	09:06:16
16	made it absolutely clear that this was	09:06:23
17	plagiarism, but since this is about teaching and	09:06:30
18	textbooks, in Germany there is a law which says	09:06:33
19	knowledge must not be prevented from being taught	09:06:39
20	by any copyrights. So he could not say whether	09:06:42
21	or not by destroying that book he would prevent	09:06:47
22	the teaching inside the book as the abstract	09:06:51
23	teaching from still being taught. The judge	09:06:54
24	suggested that we take this to the Supreme Court	09:06:58
25	because that was an open case for Germany, which	09:07:00

1	the university wouldn't do for cost, and the case	09:07:04
2	was settled that the publishing house committed	09:07:08
3	to not selling this book only selling the	09:07:13
4	already printed versions and signed a document	09:07:16
5	that this book was an infringement was	09:07:18
6	plagiarism, which was enough for me because then	09:07:23
7	I could clearly document that I wasn't the one	09:07:25
8	doing this. But this was an entirely different	09:07:28
9	kind of proceeding like we have here.	09:07:31
10	Q. Right. So in that case you were	09:07:35
11	testifying as a fact witness, a person of	09:07:37
12	knowledge of the facts as opposed to an expert	09:07:41
13	witness; is that correct?	09:07:44
14	A. So to say, yeah.	09:07:45
15	Q. Have you ever testified as	09:07:47
16	an expert in any proceedings anywhere in the	09:07:49
17	world?	09:07:53
18	A. Like this, no.	09:07:53
19	Q. Sir, when were you engaged to	09:07:54
20	assist Acqis in connection with these	09:08:00
21	proceedings?	09:08:05
22	A. This is quite a while ago. I	09:08:07
23	believe roughly October last year, September,	09:08:10
24	October last year, the exact date I do not	09:08:18
25	remember. If you wish to have that date I would	09:08:21

1	have to go through my email records which I don't	09:08:23
2	have here. I could give this to you later.	09:08:26
3	Q. Have you assisted Acqis in	09:08:29
4	connection with any of the pending litigation	09:08:36
5	matters as opposed to these two IPR proceedings?	09:08:37
6	A. No. Not as far as these documents	09:08:40
7	go or anything, no.	09:08:48
8	Q. Have you reviewed any confidential	09:08:50
9	information of the petitioner EMC that was	09:08:54
10	produced in the litigation?	09:09:00
11	A. No.	09:09:01
12	Q. Have you reviewed any confidential	09:09:02
13	information of Alcatel-Lucent from the	09:09:04
14	Acqis-Alcatel-Lucent litigation?	09:09:13
15	A. I am not aware having seen that or	09:09:16
16	even having heard about that. I am aware that	09:09:17
17	there are things like that ongoing, but this is	09:09:20
18	entirely out of the scope of my work here and the	09:09:25
19	context in which we performed that work.	09:09:27
20	Q. Right and I'm just trying to get	09:09:29
21	an understanding of what you did or didn't review	09:09:34
22	since your engagement, so that's why I asked the	09:09:37
23	question whether you had reviewed any	09:09:41
24	confidential information of either EMC or	09:09:43
25	Alcatel-Lucent. And so the answer is no, you	09:09:45

1	have not?	09:09:48
2	A. But for my understanding this is	09:09:49
3	confidential information, it would be not even	09:09:51
4	okay to give it to me, right?	09:09:54
5	Q. Well	09:09:59
6	A. You're kind of asking me whether I	09:10:01
7	wrongfully saw a document.	09:10:03
8	Q. No, there are Protective Orders in	09:10:04
9	the litigation that enable experts engaged by	09:10:06
10	Acqis to see information, and we're not aware	09:10:10
11	that you were provided information, but that's	09:10:14
12	why I wanted to confirm you were not provided	09:10:17
13	information under the terms of that Protective	09:10:19
14	Order?	09:10:21
15	A. No.	09:10:24
16	Q. No.	09:10:25
17	(Brief off-the-record discussion.)	09:12:49
18	BY MR. BUROKER:	09:12:54
19	Q. It looks like you've got copies,	09:12:54
20	and maybe these are the exact same things, but I	09:12:56
21	was going to provide you copies with	09:12:58
22	A. Then I will take both, that's	09:12:58
23	fine.	09:12:58
24	Q Acqis Exhibit 2021 in both	09:13:01
25	proceedings, so there's two different documents	09:13:04

1	but it's 2021 from the 1469 proceeding and 2021	09:13:06
2	from the 1462 proceeding as well. And I think	09:13:12
3	they're probably the same as what you have.	09:13:16
4	Do you need a copy?	09:13:18
5	MR. DAVIS: Do you have the super nice	09:13:20
6	bound one? If you do, I would love that. Thank	09:13:24
7	you.	09:13:26
8	MR. BUROKER: I don't know how nice	09:13:32
9	they are, but	09:13:34
10	MR. DAVIS: Thank you.	09:13:35
11	BY MR. BUROKER:	09:13:35
12	Q. So you recognize these two	09:13:41
13	documents as printouts of the declaration that	09:13:43
14	you signed and submitted in connection with the	09:13:49
15	two proceedings? And I'm not giving you a -	09:13:50
16	test. I'll represent that we believe they're	09:13:56
17	full copies of each.	09:13:58
18	A. With this disclaimer absolutely,	09:14:01
19	yes, I recognize them.	09:14:03
20	Q. How were these documents drafted?	09:14:04
21	Did you write all the words in the document?	09:14:17
22	A. I did not write all the words in	09:14:20
23	there, hardly ever do that. I mean I've reviewed	09:14:22
24	all the material and we have come to conclusions,	09:14:31
25	there have been discussions with Cooley and the	09:14:37

1	documents were jointly written. I have reviewed	09:14:41
2	them several times very carefully, I have read	09:14:44
3	them, both of them, all 250 altogether pages.	09:14:47
4	Let me see the first one is about, I believe,	09:14:52
5	roughly 100 pages, 93, plus an appendix, the	09:14:54
6	other is 114, something like that, 111. I	09:14:59
7	carefully read them to make sure that everything	09:15:03
8	in there is correct and I still believe so today	09:15:07
9	except for some very minor typos which we found,	09:15:12
10	a few commas and so forth, nothing which really	09:15:16
11	has any effect on the content of these documents.	09:15:20
12	Q. So you worked together with	09:15:24
13	Acqis's counsel at Cooley to draft these	09:15:27
14	materials but you reviewed them and signed them	09:15:30
15	as your statement, correct?	09:15:34
16	A. Well, I mean the message in here,	09:15:35
17	this is from is mine, right? And they helped,	09:15:38
18	of course, to do a lot of the detail work, for	09:15:47
19	example make sure all the references are right.	09:15:51
20	Q. And were you compensated for your	09:16:01
21	time in connection with these two proceedings?	09:16:03
22	A. Yes.	09:16:07
23	Q. Okay. And what is the hourly rate	09:16:07
24	at which you were being compensated?	09:16:09
25	A. €250.	09:16:11

1	Q. Per hour, correct?	09:16:13
2	A. Yeah.	09:16:17
3	Q. How many hours have you spent	09:16:18
4	since your engagement to date on this effort?	09:16:23
5	A. I would have to look up my	09:16:28
6	records, I don't remember the exact number.	09:16:32
7	Altogether, up to date, 50 hours, maybe 60, let's	09:16:35
8	say, plus or minus 10, 20 percent. If you want	09:16:44
9	the exact number I would have to check my	09:16:48
10	records.	09:16:51
11	Q. Approximate is fine.	09:16:53
12	Do you recall how much time you worked	09:16:59
13	on each of the two different declarations?	09:17:01
14	Roughly 50/50?	09:17:05
15	A. That I can't tell. A lot of	09:17:08
16	material is relevant for both and, as you	09:17:12
17	noticed, there is quite a bit of similarity	09:17:17
18	between these two documents, so it is hard to say	09:17:19
19	how to break this up between the two.	09:17:23
20	Q. And what did you do to prepare for	09:17:28
21	your deposition today?	09:17:34
22	A. You mean after submitting these	09:17:38
23	documents?	09:17:39
24	Q. Correct.	09:17:40
25	A. I read them several times again to	09:17:44

1	refresh my memory. I read the patents, the prior	09:17:47
2	arts not every page, there's a lot of material.	09:17:55
3	And I had a few discussions with Cooley to tell	09:17:59
4	me how this is working because this is obviously	09:18:07
5	different from a normal conversation.	09:18:11
6	Q. And how many times did you meet	09:18:14
7	with counsel for Cooley to prepare for your	09:18:19
8	deposition? So just the conversations you had	09:18:21
9	with them relating to preparing for today. And I	09:18:25
10	don't want to know the substance, you know, I	09:18:31
11	just want to know how many times.	09:18:33
12	A. Now, I didn't really try to keep	09:18:40
13	track of this particular element, so I have to	09:18:42
14	rethink this and this will not be a very accurate	09:18:44
15	answer. Three, four times.	09:18:48
16	Q. Well, those three or four times	09:18:52
17	were some of them on the telephone and were some	09:18:57
18	of them in person or were they all in person?	09:19:00
19	A. When we are getting close, in	09:19:02
20	person.	09:19:03
21	Q. And in total how many hours would	09:19:04
22	you say you spent to prepare for the deposition	09:19:07
23	over the course of those three or four meetings?	09:19:10
24	Estimates are fine.	09:19:19
25	A. Fifteen. Maybe 20, maybe less. I	09:19:21

1	mean that relates now to the question of the	09:19:24
2	total amount of time I spent and the more	09:19:27
3	detailed numbers you try to make me give, the	09:19:30
4	more the sum will possibly not match because all	09:19:32
5	the errors will become larger and larger.	09:19:36
6	Q. In your declarations you	09:19:41
7	identified material that you considered, starting	09:19:44
8	I mean in both of the declarations	09:19:49
9	approximately it's on page 5. Well, 3, 4 and 5.	09:19:52
10	Since you submitted these declarations,	09:20:01
11	in the course of preparing for your deposition,	09:20:03
12	did you review any additional materials beyond	09:20:06
13	what's listed?	09:20:09
14	A. At this moment nothing comes to my	09:20:13
15	mind. I don't think so.	09:20:15
16	Q. Did you have any communications	09:20:19
17	with anybody? After the declarations were	09:20:21
18	submitted but before your deposition, did you	09:20:27
19	have any communications with anybody other than	09:20:29
20	counsel to prepare for your deposition?	09:20:30
21	A. No, I don't think so. I don't	09:20:34
22	remember any.	09:20:37
23	Q. You never spoke to Dr. Chu, for	09:20:37
24	example, of Acqis?	09:20:41
25	A. No.	09:20:43

1	Q. You didn't speak to any of your	09:20:43
2	colleagues associated with what's called the	09:20:44
3	Bogaerts reference?	09:20:46
4	A. After the submission I did not,	09:20:49
5	and I believe we have a non-disclosure agreement	09:20:50
6	with Cooley so I even can't do that, right? I	09:20:55
7	mean this proceeding is confidential, I can't	09:21:00
8	talk to anybody. This whole context.	09:21:04
9	Q. All right, but you didn't talk to	09:21:06
10	anybody?	09:21:07
11	A. (The witness shook his head.)	09:21:10
12	Q. Did you also review the Patent	09:21:17
13	Owner Response filed by Acqis that was submitted	09:21:21
14	to the Patent and Trademark Office at the same	09:21:25
15	time at your declarations?	09:21:28
16	A. I have read that, both responses	09:21:30
17	for both patents and yeah.	09:21:32
18	Q. Did you review them before they	09:21:36
19	were submitted to the Patent and Trademark	09:21:38
20	Office?	09:21:40
21	A. I'm not quite sure. I may have	09:21:46
22	seen an early version. I'm quite sure I have not	09:21:50
23	seen the final version and if so it was very late	09:21:53
24	anyway.	09:21:59
25	Q. You are aware that those Patent	09:22:02

1	Owner Responses cite to your declarations,	09:22:04
2	correct?	09:22:08
3	A. Yeah.	09:22:09
4	Q. And did you believe when you	09:22:10
5	reviewed the Patent Owner's Response that the	09:22:14
6	citations to your declaration were fair	09:22:18
7	representations of your declarations?	09:22:21
8	A. Yes, I believe so.	09:22:24
9	Q. Okay. Was there anything in the	09:22:26
10	Patent Owner's Responses that you didn't agree	09:22:31
11	with?	09:22:33
12	A. I don't remember anything at this	09:22:33
13	point.	09:22:35
14	Q. In preparing your declarations,	09:22:35
15	outside of attorneys for Cooley just so I've	09:22:44
16	got a clear record, I'm not sure if I got a clear	09:22:47
17	record, it was my fault in preparing the	09:22:49
18	declarations, other than counsel for Cooley, did	09:22:52
19	you speak to anybody else to gain facts or	09:22:54
20	information to help you make your declaration in	09:22:58
21	this case?	09:23:00
22	A. I only contacted one person in	09:23:07
23	this context and that is Hans Müller who is	09:23:09
24	co-author on the RD24, on the, as you call it,	09:23:17
25	Bogaerts reference about his recollection of the	09:23:20

1	public dissemination of that document. That was	09:23:26
2	all.	09:23:29
3	Q. Did you mention that you spoke to	09:23:29
4	Dr is it Dr. Müller or is he mister?	09:23:31
5	A. Doctor.	09:23:35
6	Q. Doctor. Did you mention that	09:23:36
7	you'd spoken to Dr. Müller in your declaration?	09:23:37
8	I didn't see it.	09:23:43
9	A. I believe not. I tried to get	09:23:44
10	something concrete from him, I didn't, so there	09:23:48
11	wasn't any point mentioning it.	09:23:51
12	Q. What did you try to get that was	09:23:53
13	concrete from him?	09:23:54
14	A. Whether he remembered the exact	09:23:56
15	date when it was put on to the CERN internet so	09:23:58
16	that it was accessible to everybody.	09:24:04
17	Q. He could not remember?	09:24:07
18	A. No.	09:24:10
19	Q. And he didn't have any information	09:24:10
20	that he provided to you that would say one way or	09:24:12
21	the other when it was put on that server?	09:24:15
22	A. The message was, "It's almost	09:24:22
23	20 years ago, how could I remember?" And, I	09:24:24
24	mean, I put forth in my declaration quite a bit	09:24:28
25	of text, and maybe we should go through this,	09:24:33

1	what we can say, what we cannot say and so forth.	09:24:37
2	This is what basically came out of that.	09:24:40
3	Q. One question about the materials	09:24:43
4	you did consider. One of them, the item that's	09:24:52
5	listed in both declarations is the 2012 Federal	09:24:55
6	Circuit Bar Association Model Patent Jury	09:24:59
7	Instructions. Do you recall why you looked at	09:25:02
8	those?	09:25:04
9	A. In order to understand what	09:25:06
10	principles are to be applied and I mean this is	09:25:09
11	one of the reasons why I put all of this into	09:25:14
12	this document to make clear what are the	09:25:17
13	principles which we had used in the analysis in	09:25:19
14	this declaration.	09:25:22
15	Q. You understand that these two	09:25:24
16	Acqis patents are part of a large family of	09:25:28
17	patents that is owned by Acqis; is that correct?	09:25:31
18	Do you understand that?	09:25:34
19	A. Yes.	09:25:35
20	Q. You didn't list having reviewed	09:25:35
21	any of the other patents or patent	09:25:40
22	file histories; is that correct?	09:25:43
23	A. Well, the list is quite long,	09:25:45
24	we would have to go through this but if you say	09:25:46
25	so I believe you.	09:25:48

1	Q. Do you know why you didn't look at	09:25:53
2	any materials from any of the related patents or	09:25:55
3	file histories?	09:25:59
4	A. I mean I was asked to form	09:26:00
5	an opinion about the case raised against these	09:26:04
6	two patents, whether or not they are valid or not	09:26:08
7	valid and this is what I did. And for my	09:26:11
8	analysis I used everything which I thought was	09:26:15
9	relevant and this didn't seem to be relevant in	09:26:18
10	order to also limit the amount of time which went	09:26:26
11	into this.	09:26:29
12	Q. For both declarations I noticed	09:26:33
13	that you did not provide a copy of your CV; is	09:26:37
14	that correct?	09:26:37
15	A. There is a short version of it in	09:26:43
16	here under Section II, for instance, in the	09:26:54
17	Document 01462, this is the '873 Patent,	09:26:56
18	professional qualifications, and there is	09:27:05
19	a similar one in the other one, which basically	09:27:07
20	says most of the things which I've done. It's a	09:27:11
21	high-level CV, if you want more details it's	09:27:15
22	relatively long you can have them. But we did	09:27:18
23	not include what is usually done like the most	09:27:22
24	important publications, patents filed and stuff	09:27:25
25	like that, because it didn't appear to be	09:27:28

1	relevant.	09:27:29
2	Q. Okay. I just wanted to confirm	09:27:30
3	that your CV was not attached as an exhibit and	09:27:34
4	what we have for your professional qualifications	09:27:36
5	in each proceeding is what you've provided in	09:27:39
6	Section II of your declaration; is that fair?	09:27:43
7	A. Yeah. Is there anything more you	09:27:46
8	like to know?	09:27:48
9	Q. No, I just trying to make clear	09:27:49
10	for the record what we have and what we don't	09:27:51
11	have at this point.	09:27:54
12	So in 1998 you had already received your	09:27:58
13	PhD in nuclear physics from Frankfurt University;	09:28:03
14	is that correct?	09:28:03
15	A. Yes. That was in 1993. I	09:28:10
16	graduated in 1993 and right after that I moved to	09:28:13
17	Lawrence Berkeley National Laboratory as	09:28:18
18	a so-called post-doc. I got a Humboldt	09:28:21
19	Fellowship, which is an award which basically	09:28:24
20	says, "Here's a bunch of money, do what you want	09:28:27
21	with it", it's quite nice. And although I have	09:28:29
22	a PhD in nuclear physics, I have the Humboldt	09:28:35
23	Fellowship in computer science, which is	09:28:40
24	untypical. I had a dual interest all my life and	09:28:43
25	my thesis is also it is nuclear physics, but	09:28:48

1	for it to be done it needed a quite big and	09:28:53
2	distributed computer to be built and it was	09:28:56
3	built, it worked, and with that working computer,	09:28:59
4	the data was recorded and that data was then	09:29:01
5	analyzed and for the analyzed data I got the	09:29:05
6	physics degree. And I did a Rigorosum, which	09:29:07
7	means there were three exams, one hour each,	09:29:14
8	theoretical physics, experimental physics and	09:29:20
9	computer science, which all had to be passed.	09:29:23
10	Q. Much of that answer is helpful but	09:29:37
11	I was just trying to get to a simple point. So,	09:29:39
12	by 1998, you had your PhD in nuclear physics from	09:29:42
13	Frankfurt University which you'd received in	09:29:46
1.4	1993; is that correct?	09:29:49
15	A. That is correct.	09:29:50
16	Q. And nuclear physics is the study	09:29:51
17	of what exactly, at a very high level?	09:29:54
18	A. This kind of instruction is not	09:29:57
19	ease. But Goethe used to say to understand what	09:30:07
20	keeps things together at its most fundamental	09:30:12
21	level. So nuclear physics tries to understand	09:30:15
22	the fundamental forces of nature of which there	09:30:21
23	are four but normal people only experience two,	09:30:22
24	gravitation and electric force, try to understand	09:30:29
25	what happens inside a nucleus. In our case we	09:30:36

1	tried to understand what happens at the Big Bang	09:30:40
2	and why do we exist, rather fundamental	09:30:42
3	questions. The principle behind that is all	09:30:46
4	these experiments are rather large systems, we're	09:30:51
5	talking at that time already millions of sensors	09:30:57
6	read out at megahertz rate and that means no	09:31:02
7	ordinary storage media could take such data and	09:31:07
8	that requires a large amount of computer	09:31:11
9	infrastructure to be in place so absorb that data	09:31:14
10	and analyze that data. And that is one of the	09:31:18
11	reasons why I chose that field because I had	09:31:22
12	an area which really, really required the most	09:31:24
13	cutting-edge computer infrastructure, computer	09:31:27
14	architectures to do the job. Nothing could be	09:31:32
15	purchased off the shelf. Sloppy spoken, it's	09:31:34
16	a nice playground for somebody who's really	09:31:41
17	interested in computer science.	09:31:44
18	My reason for answering your other	09:31:46
19	question in a longer form was since you're	09:31:50
20	emphasizing the PhD in nuclear physics, it might	09:31:53
21	seem that I'm not an expert in computer science	09:31:56
22	and this is why I tried to make that clear. And,	09:31:58
23	as you see, although I have a PhD in nuclear	09:32:01
24	physics, the next thing that happened was I was	09:32:04
25	offered a chair in computer science, which is not	09:32:06

1	very usual.	09:32:10
2	Q. Okay, just to confirm, you do not	09:32:12
3	have a degree in computer science, correct? Your	09:32:15
4	degree is in nuclear physics even though you've	09:32:17
5	studied computer science?	09:32:21
6	A. I'm full Professor, endowed full	09:32:22
7	Professor in computer science, so	09:32:25
8	Q. But your degree is not in computer	09:32:27
9	science; is that right?	09:32:30
10	A. The PhD degree, yes.	09:32:31
11	Q. Well your undergraduate degrees	09:32:32
12	were not in computer science either were they?	09:32:35
13	A. The undergraduate degree is	09:32:39
14	physics, too. It's solid state physics, it's	09:32:39
15	about scanning tunneling microscopy, but it may	09:32:42
16	be surprising to you the scanning tunneling	09:32:48
17	microscope needed a computer to record the data	09:32:52
18	and an image analysis system to recalculate the	09:32:52
19	highly noisy signals which were recorded and I	09:32:56
20	built that system. So, again, I coupled computer	09:33:00
21	engineering/computer science with the	09:33:03
22	requirements in physics. It is always nicer to	09:33:06
23	build something which somebody needs than like	09:33:11
24	often happens some theoretical work is being done	09:33:16
25	but nobody has a real application for using it.	09:33:19

1	Relevance.	09:33:24
2	Q. Okay. But you mentioned computer	09:33:25
3	engineering, also you did not get a degree in	09:33:28
4	computer engineering what you're saying is you	09:33:35
5	took courses and studied that as part of the work	09:33:36
6	that you were doing in the physics field,	09:33:39
7	correct?	09:33:42
8	A. Yes, most of it is self-trained.	09:33:43
9	Q. Good. So then in paragraph 15	09:33:45
10	and most of my questions are based on the '814	09:33:52
11	declaration, so the paragraph numbers might get	09:33:58
12	off if we use something else so the '814	09:34:00
13	declaration, paragraph 15, you offer your view of	09:34:03
14	what a person of skill in the art is for that	09:34:11
15	patent. Do you see that?	09:34:13
16	A. I pulled it up, yes.	09:34:15
17	Q. And a concept of a person of skill	09:34:15
18	in the art is based on your understanding	09:34:17
19	provided by counsel about what that means in the	09:34:21
20	patent law; is that correct. In paragraph 13,	09:34:24
21	for example, you explain what you understand a	09:34:28
22	person of skill in the art to be?	09:34:32
23	A. Let me look at it real quickly.	09:34:35
24	Q. Sure. And to be fair,	09:34:37
25	paragraph 14 also then explains what you	09:34:48

1	understand to be the appropriate level of the	09:34:50
2	skill in the art, so I don't want to leave that	09:34:53
3	one out. So it's 13, 14 and 15 sort of together.	09:34:55
4	A. Yes. Bachelor's degree, with	09:34:58
5	a bit of focus on computer architecture, yes.	09:35:01
6	Q. And why did you choose bachelor's	09:35:06
7	degree in computer science for the '814 Patent as	09:35:12
8	opposed to other fields like physics or computer	09:35:16
9	engineering?	09:35:19
10	A. Kind of obvious. This patent	09:35:21
11	family relates to computer architecture.	09:35:24
12	Although I should say it relates to parallel	09:35:27
13	computer architecture and my understanding is,	09:35:30
14	and that was confirmed by Cooley and I also	09:35:33
15	believe I have read that in the declaration by	09:35:36
16	Young, that this is the kind of level which is	09:35:39
17	typically being used. So, you know, it can't be	09:35:42
18	too high a level. It has to be an ordinary skill	09:35:46
19	in the art type thing and that is what I	09:35:53
20	understand has been considered as the typical	09:35:56
21	level.	09:35:59
22	Q. Okay. It says in the middle, the	09:36:00
23	person would hold a bachelor's degree or the	09:36:06
24	equivalent in computer science or related	09:36:09
25	academic field. What's your understanding of	09:36:13

1	what "related academic field" is?	09:36:15
2	A. This area, particularly when it is	09:36:19
3	about computer architecture, has quite a few ties	09:36:24
4	to engineering and computer engineering and you	09:36:29
5	see that in particular since many of the schools	09:36:34
6	in the U.S. even call themselves CSE/EE, Berkeley	09:36:38
7	is an example, computer science/computer	09:36:45
8	engineering. So that would be one example for	09:36:47
9	a related field. But the fundamental knowledge	09:36:49
10	which is required has a very has a strong	09:36:56
11	element of computer science, right? I mean you	09:37:00
12	have to understand how a computer works, how the	09:37:02
13	different bits and pieces interrelate to each	09:37:05
14	other, what are the appropriate standards in	09:37:10
15	there being used, what are the principles to be	09:37:11
16	used for what works, what doesn't work. And this	09:37:13
17	is usually this is taught in computer science.	09:37:16
18	If it then goes into how does it work in detail,	09:37:21
19	how can it work, fast signals, slow signals,	09:37:24
20	these kind of things, then engineering comes more	09:37:27
21	and more into play.	09:37:31
22	Q. And what did you mean by "modular	09:37:35
23	computing systems" in that definition?	09:37:41
24	A. Let me just check where is it?	09:37:48
25	Q. Two lines down where we were	09:37:51

1	looking:	09:37:52
2	" and three to four years of	09:37:53
3	additional experience in the field of modular	09:37:57
4	computer systems"	09:38:03
5	A. Yes, I see. Many of the	09:38:05
6	references which are being discussed here include	09:38:11
7	systems which consist of different subfunctions,	09:38:16
8	subsystems. Later they are being called or have	09:38:22
9	been called nodes. So one computer, another	09:38:27
10	computer, a network in between maybe a mass	09:38:30
11	storage system somewhere elsewhere. In	09:38:34
12	particular	09:38:34
13	(The court reporter sought	09:38:34
14	clarification.)	09:38:34
15	THE WITNESS: Mass storage system.	09:38:34
16	And their interconnect matrix allows	09:38:52
17	them to be combined in many different ways, and	09:38:56
18	that means you have a modular system allowing	09:38:58
19	different combinations of things together. And	09:39:02
20	this is relatively different as compared to	09:39:05
21	monolithic systems where, for instance, one	09:39:11
22	example could be the Blue Gene family of	09:39:15
23	computers which basically come as one big system	09:39:24
24	where if you look carefully you still find the	09:39:27
25	same building blocks, but they are all engineered	09:39:29

1	together as one thing and there is no	09:39:34
2	interchangeability except you buy more nodes from	09:39:36
3	the very same thing from the same vendor.	09:39:40
4	BY MR. BUROKER:	09:39:42
5	Q. Okay. Is it correct to say that	09:39:42
6	by 1998 there were a variety of modular computing	09:39:45
7	systems, computer architectures and computer	09:39:51
8	communication protocols that were known to the	09:39:55
9	person of skill in the art?	09:39:56
10	MR. DAVIS: Objection; form.	09:40:00
11	THE WITNESS: In order to give a very	09:40:05
12	correct answer, the term "known" would have to be	09:40:16
13	differentiated. Known in the sense of aware of	09:40:20
14	existing certainly, yes. Known in the sense of	09:40:25
15	being an in-depth expert is a different thing.	09:40:28
16	This is why I hesitated to respond too quickly.	09:40:32
17	Although we say here bachelor in computer	09:40:38
18	science, the normal and I reviewed quite a few	09:40:44
19	of the curriculum and I'm teaching this since	09:40:48
20	1998 in fact, in regular classes bachelor of	09:40:52
21	computer science usually includes quite a bit of	09:41:01
22	mathematics, learning to start programming. One	09:41:04
23	has to understand where they come from, right,	09:41:07
24	they come from high school and usually they have	09:41:09
25	no knowledge, no concept of real programming,	09:41:11

1	except if you have a few geeks who did this by	09:41:15
2	themselves, like I did for example. But they	09:41:17
3	have to learn all of that, and then they learn	09:41:19
4	computer architecture but only computer	09:41:23
5	architecture in the sense of the single computer	09:41:25
6	with like one system. The entire context of	09:41:30
7	parallel systems with all the additional	09:41:36
8	complications which come in and I'm sure we	09:41:39
9	will get to that point later are not typically	09:41:42
10	part of the generic computer science curriculum.	09:41:46
11	So if you say "are known" the answer would be	09:41:52
12	they certainly knew it existed and they certainly	09:41:55
13	may have known the relevant particular buzzwords,	09:41:59
14	but the in-depth knowledge to know how a system	09:42:03
15	really works, to put such a system together,	09:42:06
16	debug it, find error, I would say likely not.	09:42:09
17	BY MR. BUROKER:	09:42:13
18	Q. Well, this person that we've	09:42:13
19	defined isn't just a beginning computer science	09:42:14
20	student, it's a person who's already received	09:42:21
21	their degree and worked for three to four years	09:42:23
22	in the field. So would that person have more	09:42:25
23	in-depth knowledge of modular computer systems,	09:42:27
24	computer architecture and communication	09:42:32
25	protocols?	09:42:33

1	MR. DAVIS: Objection; form.	09:42:33
2	THE WITNESS: Whether generic	09:42:38
3	experience working in the field at this abstract	09:42:40
4	level, the answer would be no. There would have	09:42:45
5	been some additional teaching and specialization	09:42:47
6	have to happen after the degree as a bachelor.	09:42:51
7	And maybe I should clarify that. I	09:43:01
8	mean I do teach a class about parallel computer	09:43:05
9	architecture since many years now, and this is	09:43:08
10	going a full semester, it's a full big class with	09:43:10
11	everything, and it is far not enough to get the	09:43:14
12	relevant knowledge into the heads of the students	09:43:21
13	and this is master level.	09:43:23
14	BY MR. BUROKER:	09:43:23
15	Q. In what year did you begin working	09:43:30
16	on modular computer systems, computer	09:43:33
17	architecture and computer communication	09:43:39
18	protocols? That was well before '93 I assume.	09:43:44
19	A. It's not possible to give an exact	09:43:47
20	and good date but in order to give you an answer	09:43:55
21	maybe I just tell you what I did and then you see	09:44:00
22	how things evolved. At the age of	09:44:02
23	Q. Well, I'm asking for a very	09:44:06
24	specific I know that you like to answer	09:44:07
25	questions in your way and you're welcome to, I'm	09:44:10

1	asking for a year. So, if you can answer that	09:44:12
2	question then I'm happy to have you give	09:44:15
3	an explanation.	09:44:18
4	A. My first modular and own computer	09:44:18
5	I got and improved and built was at the age of	09:44:24
6	probably 17. Now, I have to calculate the year.	09:44:28
7	You know my age so, I'm 52 years old, so at the	09:44:34
8	age of 16, this is 36 years ago, right? 2015	09:44:41
9	minus 36 we're talking something like 1980. That	09:44:53
10	was a Z80 computer, 8-bit machine. Then I later	09:44:57
11	started connecting multiple of those, building	09:45:02
12	larger systems all by myself. I financed my	09:45:06
13	studies by building computers for industry and	09:45:09
14	they paid me for it, which shows this is going	09:45:12
15	back quite some way. I already outlined doing my	09:45:17
16	diploma pieces I built such a system from	09:45:23
17	scratch. In the thesis it was a larger system	09:45:26
18	and, in fact, it is the first bigger highly	09:45:28
19	modular interconnected system I believe that was	09:45:33
20	ever built, and this is timescale '93. So it's	09:45:36
21	going back a long time.	09:45:40
22	Q. So, would you consider yourself to	09:45:44
23	be an expert in the field of modular computing	09:45:46
24	systems, computer architecture and computer	09:45:50
25	communication protocols?	09:45:53

1	A. Yes.	09:45:54
2	Q. Okay. So when you're doing your	09:45:54
3	analysis in connection with this case and	09:45:57
4	providing this declaration, were you looking at	09:45:59
5	things from your perspective as an expert, or	09:46:03
6	from the perspective of a person of skill in it	09:46:07
7	the art as you've defined it, which is someone of	09:46:08
8	less experience than you?	09:46:13
9	A. Had to be, yes. And I believe I	09:46:16
10	set this forth, I mean the definition of a person	09:46:18
11	of ordinary skill in the art is set forth in the	09:46:21
12	declaration, and my understanding is this is the	09:46:24
13	perspective which had to be used.	09:46:29
14	Q. Right. So you used the	09:46:34
15	person-of-skill-in-the-art perspective as opposed	09:46:36
16	to your own, correct?	09:46:38
17	A. Does it have to be opposed to?	09:46:42
18	Q. Well, in analyzing the opinions,	09:46:46
19	whether something is obvious or anticipated or	09:46:50
20	known, did you do that from the perspective of	09:46:53
21	a person of skill in the art or from an expert's	09:46:56
22	perspective?	09:47:01
23	A. Now I understand the subject	09:47:07
24	material of course as an expert. The conclusions	09:47:08
25	drawn in here I believe are valid in both cases,	09:47:12

1	and we can go into details, but in principle they	09:47:17
2	would have to be would be taken in the view of	09:47:22
3	the person of ordinary skill in the art because	09:47:25
4	this is how it works.	09:47:28
5	Q. So what I've handed you is what we	09:48:58
6	call the Bogaerts reference which is Exhibit 1011	09:49:01
7	in the 1469 IPR proceeding which is the one	09:49:08
8	related to the '814 Patent. Make sure I have the	09:49:14
9	numbers right, there are a lot of complicated	09:49:25
10	numbers here.	09:49:27
11	So, are you familiar with this document?	09:49:28
12	A. Yes, I am.	09:49:30
13	Q. Okay. And, in fact, if you look	09:49:31
14	at I'm going to have you do two things at once	09:49:34
15	paragraph 170 of the '814 declaration which	09:49:40
16	you were just looking at, the first sentence	09:49:44
17	says:	09:49:48
18	"I am an author of the Bogaerts	09:49:49
19	reference."	09:49:52
20	Is that correct?	09:49:52
21	A. Yes, as you can see on the front	09:49:53
22	page.	09:49:55
23	Q. In other places I think you also	09:49:55
24	say you're a co-author but you basically mean	09:49:57
25	you're one of the authors, correct?	09:50:00

1	A. Yeah. There is only a very minor	09:50:03
2	distinction between the two and that is more	09:50:09
3	a game played in research of who is called the	09:50:14
4	primary or first author and who is called the	09:50:17
5	last author and that even is different in the	09:50:19
6	different fields. So in medicine the last author	09:50:21
7	is always the group leader. Here this is	09:50:24
8	a status report and basically there is just	09:50:29
9	basically a list of those who have contributed.	09:50:32
10	Q. That's what I wanted to get to.	09:50:38
11	Was there a primary author of this status report?	09:50:40
12	A. The way it worked was this is	09:50:46
13	a status report of a working group, this RD24,	09:50:52
14	which was chaired by Hans Müller and he did the	09:50:55
15	writing most of the time, putting things together	09:50:57
16	where everybody delivered bits and pieces. So I	09:51:01
17	certainly delivered also some chapters here, in	09:51:05
18	particular about the PCI-SCI bridge. Then it was	09:51:07
19	circulated and at some point everybody said it's	09:51:11
20	okay to be our status report at this particular	09:51:14
21	time.	09:51:19
22	Q. Did everyone on the front page of	09:51:23
23	this document contribute to the text of the	09:51:25
24	status report?	09:51:30
25	A. I certainly did. I can't tell for	09:51:33

1	everyone in particular because, you know, I	09:51:35
2	haven't checked every email which went possibly	09:51:38
3	directly to Hans Müller, but certainly everybody	09:51:42
4	was involved here. I know most of the people	09:51:46
5	personally, actually I know all of them pretty	09:51:50
6	much, although many have disappeared from this	09:51:54
7	research field.	09:51:59
8	Q. So how was this document compiled?	09:51:59
9	You mentioned emails. How did it get to be in	09:52:01
10	the form that it's in?	09:52:05
11	A. I remember Hans Müller likes to	09:52:10
12	write with FrameMaker, which is a text writing	09:52:13
13	tool, I'm not sure it exists anymore, quite	09:52:17
14	a nice thing. I believe at that time I had	09:52:21
15	FrameMaker, too. And the important thing was are	09:52:26
16	the results we can present which are convincing,	09:52:33
17	showing that there was great progress? These	09:52:36
18	results were pulled together, sent forth and	09:52:40
19	back. I mean you have to understand I was in	09:52:45
20	Berkeley, California, this is nine hours' time	09:52:48
21	difference. I spent frequent time at CERN at	09:52:49
22	that time going constantly forth and back.	09:52:52
23	Andreas Bogaerts is CERN.	09:52:57
24	We have the University of Oslo, Bernard	09:53:00
25	Skaai he's retired now. Oslo is a two- or	09:53:03

1	three-hour flight from Geneva, so for them it was	09:53:10
2	also quite an effort to get there, they did a lot	09:53:13
3	of their work at Oslo.	09:53:15
4	Spain. We had a student who worked at	09:53:18
5	CERN but the group leader was in Spain so, again,	09:53:25
6	requirement for interchange.	09:53:29
7	Kare Løchsen and Hugo Kohmann is	09:53:31
8	Dolphin, again same thing. Dolphin's role was	09:53:34
9	the supplier of many of the chips which are being	09:53:38
10	discussed in here and being evaluated, tested and	09:53:42
11	so forth, being part of a	09:53:47
12	Digital Equipment is head of joint	09:53:50
13	project with CERN and I believe this is the	09:53:53
14	Geneva branch of Digital so he was close. He	09:53:55
15	could have had direct interactions with Hans	09:53:58
16	Müller.	09:54:02
17	Q. Right, so the question that I	09:54:02
18	asked was more, you know, was there a person who	09:54:04
19	typed in all the text or did each of the various	09:54:08
20	people send sections to be posted into the	09:54:10
21	document? How was it compiled?	09:54:13
22	A. Both. I mean this is almost	09:54:16
23	20 years ago.	09:54:20
24	Q. Right.	09:54:21
25	A. But this was nothing out of the	09:54:21

1	ordinary, and the normal way it goes is people	09:54:24
2	send in stuff, text blocks, figures, diagrams.	09:54:27
3	I'm quite sure this diagram is from myself. The	09:54:32
4	big picture I believe Hans Müller did, although	09:54:35
5	the board I believe is the one I supplied. You	09:54:38
6	know, these kind of details. And then Hans	09:54:42
7	Müller put it together in a big document, then we	09:54:46
8	went over it, and at some point it was the final	09:54:48
9	version, a postscript file was generated and this	09:54:50
10	is what was submitted.	09:54:54
11	Q. So based on your recollection,	09:54:55
12	which portions of this document did you write or	09:55:00
13	which figures did you contribute?	09:55:03
14	MR. DAVIS: Objection; form.	09:55:07
15	THE WITNESS: I mean, this is really a	09:55:14
16	long time ago. My focus of work at that time was	09:55:17
17	the PCI-SCI adapter, which you may have noticed	09:55:25
18	is a core device in this whole document, because	09:55:29
19	many of the system architectures which are	09:55:32
20	sketched and outlined here need this as	09:55:36
21	a fundamental building block. And I was	09:55:39
22	basically working with very a significant	09:55:43
23	fraction of my time on this device because I	09:55:47
24	needed it for myself in Berkeley. We were trying	09:55:49
25	to build a very large data acquisition system and	09:55:52

1	we needed the PCI-SCI device for that. So that	09:55:55
2	means Section 3.1 is a very strong candidate for	09:55:58
3	me being involved. You also see that there is a	09:56:06
4	small 3.2 says, "Collaboration with the	09:56:11
5	STAR Trigger group", which is me basically. STAR	09:56:15
6	is the name of an experiment being prepared at	09:56:21
7	that time at Brookhaven National Laboratory.	09:56:23
8	STAR stands for solenoidal tracker at RHIC.	09:56:28
9	S-o-l-e-n-o-i-d-a-l tracker at RHIC. A solenoid	09:56:34
10	is a particular kind of a magnet.	09:56:43
11	BY MR. BUROKER:	09:56:50
12	Q. So, at least and there may be	09:56:50
13	others but you recall at least contributing to	09:56:52
14	3.1 and 3.2?	09:56:58
15	A. These would be the core ones. I	09:56:59
16	have been involved in other stuff. I have	09:57:01
17	certainly read it and looked at it, but I can't	09:57:03
18	remember the details after such a long time.	09:57:11
19	Q. This document talks about two	09:57:15
20	different PCI-SCI adapters, correct? There's the	09:57:22
21	CERN one which you mentioned and then there's	09:57:26
22	also one by Dolphin; is that right?	09:57:28
23	A. Correct.	09:57:31
24	Q. Did you work on the Dolphin	09:57:31
25	PCI-SCI adapter?	09:57:33

1	A. No. I believe at that time it	09:57:35
2	didn't really fully exist yet. Let me just	09:57:39
3	check. Do you remember which section it is being	09:57:45
4	discussed? Here we are.	09:57:49
5	Q. Where are you looking?	09:57:59
6	A. Section 3.3, it says:	09:58:00
7	"RD24 has acquired Dolphin bridges"	09:58:03
8	Not sure it existed yet or what state	09:58:23
9	it was at that time.	09:58:25
10	Q. Okay. How did you come to be	09:58:31
11	involved in this RD24 project?	09:58:47
12	A. I need to outline what this is all	09:58:55
13	about in order to make this clear.	09:58:58
14	"RD" stands for "research and	09:59:00
15	development" and 24 simply means it's the 24th	09:59:02
16	research and development project at CERN. This	09:59:06
17	nuclear physics or high-energy physics field has	09:59:11
18	a particular problem. It takes some often	09:59:15
19	25 years to prepare an experiment, this long, and	09:59:21
20	at the LHC we're talking about that kind of time.	09:59:25
21	The LHC was first started to be planned around	09:59:30
22	1980, the first proposals, the first documents,	09:59:33
23	how it was going to be were written at that time,	09:59:36
24	and it went in operation 2007/8/9, I can't	09:59:39
25	remember exactly. 2005 it was scheduled but	09:59:47

1	there were delays. And when it was started,	09:59:49
2	there were many areas where the proposal	09:59:54
3	basically said today no known technologies exist	09:59:58
4	to solve the problem, in particular in computer	10:00:01
5	engineering areas. Everybody likes to refer to	10:00:05
6	Moore's law like things will get faster and	10:00:08
7	cheaper but, of course, over a period of 25 years	10:00:13
8	we're talking at the least three, four computer	10:00:15
9	generations, it is rather difficult to make	10:00:19
LO	a clear, dependable proposal that how it would be	10:00:21
L1	to build such a system and how much it would cost	10:00:24
12	because when you submit a proposal you have to	10:00:27
13	have a cost figure. So in order to avoid either	10:00:29
L 4	using hopelessly dated technology when the	10:00:34
L5	experiment went online and, I mean, the LHC	10:00:37
16	project all together is a \$6 billion project,	10:00:40
L7	it's not a cheap thing there had to be	10:00:43
L 8	research and development done in order to	10:00:47
L 9	minimize the risk of uncertainty which technology	10:00:53
20	to use and that the technology would still be	10:00:55
21	available when the experiment and the accelerator	10:00:57
22	would go online. Lots of technologies come and	10:01:01
23	go. And RD24 is the research and development	10:01:03
24	project which was set forth to investigate and	10:01:08
25	develop a modular, highly scaleable computer	10:01:11

1	architecture, scaling to literally thousands of	10:01:14
2	computer nodes. The CERN experiments today have	10:01:17
3	thousands of computers connected together to	10:01:20
4	process the data of each and every experiment	10:01:23
5	there, huge effort, it would fill the entire	10:01:25
6	building, yeah? And there was no network	10:01:30
7	existing which would solve these problems, so	10:01:34
8	RD24 decided to focus on SCI the scalable	10:01:40
9	coherent interface as a very good and strong	10:01:44
10	candidate for solving these problems. So this is	10:01:46
11	the context.	10:01:49
12	I was working at that time in Berkeley,	10:01:50
13	for the STAR experiment at the Relativistic Heavy	10:01:53
14	Ion Collider in Brookhaven.	10:02:06
15	(The court reporter sought	10:02:06
16	clarification.)	10:02:06
17	THE WITNESS: Relativistic Heavy Iron	10:02:08
18	Collider. Relativistic stands for that the	10:02:10
19	particles basically have speed of light. And	10:02:11
20	same problem, long-term development, yet	10:02:15
21	requirement to make clear proposals how one could	10:02:21
22	actually handle this kind of amount of data.	10:02:25
23	When I started in Berkeley, I was asked	10:02:28
24	to do a technology evaluation to look at ATM, at	10:02:32
25	fibre channel f-i-b-r-e channel the English	10:02:38

1	spelling, the technology uses that and SCI.	10:02:43
2	I discarded ATM for making no sense, I	10:02:48
3	didn't like fibre channel, and focused on SCI.	10:02:52
4	So it was obvious that we work together with the	10:02:55
5	people doing the same thing at CERN. The amount	10:02:57
6	of R&D which was necessary was just way too much	10:03:03
7	to be done by a small group all by itself. So,	10:03:07
8	we joined forces basically.	10:03:10
9	BY MR. BUROKER:	10:03:13
10	Q. Did you already know Dr. Müller	10:03:13
11	before you got involved or who was your point of	10:03:17
12	contact when you first got involved with the RD24	10:03:20
13	project?	10:03:25
14	A. I'm not 100 percent sure. The	10:03:30
15	problem is I am affiliated with CERN since I'm	10:03:32
16	a PhD student. CERN use technology I developed	10:03:38
17	while I was already at GSI and used it for the	10:03:41
18	CERN experiments. So I have a CERN user ID and I	10:03:43
19	could go there any time and I retained that when	10:03:47
20	I was in Berkeley.	10:03:50
21	My best guess is that Dave Gustafson,	10:03:53
22	the author and Chair of the SCI Committee, the	10:04:00
23	SCI standard who was indirectly involved in	10:04:04
24	this as well but he wasn't a member of the	10:04:07
25	working group and therefore is not author on this	10:04:09

1	document may have said, "Hey, do you know	10:04:11
2	there is a group, wouldn't it make sense for you	10:04:13
3	to be involved?" It may also be that I just	10:04:16
4	that we already had something to do earlier.	10:04:25
5	I would really have to check my records more than	10:04:28
6	20 years ago, I'm not sure I still have all the	10:04:30
7	emails. But in this area, this is a highly	10:04:32
8	specialized very high-tech, cutting-edge field,	10:04:38
9	the community is small and they are usually	10:04:45
10	and we had, too, certain kinds of conferences,	10:04:51
11	working meetings and so forth, so it was almost	10:04:53
12	clear that we had to bump into each other and	10:04:58
13	then decide that it makes sense to work together.	10:05:00
14	Q. So you mentioned that you were	10:05:05
15	helping to develop what you mentioned in the	10:05:07
16	document as the CERN PCI-SCI adapters. Did any	10:05:10
17	of the other people on this document help you	10:05:14
18	with that?	10:05:16
19	A. The part of this document I don't	10:05:23
20	like is the CERN PCI-SCI adapter because the	10:05:26
21	majority of the work I have done myself. But,	10:05:30
22	yes, there has been cooperation and I remember I	10:05:33
23	spent something like close to two months at CERN,	10:05:37
24	when we decided, "We are rather close, let's do	10:05:41
25	some real push together", but I can't tell	10:05:46

1	whether this was before or after the submission	10:05:49
2	of this report because if you know you may	10:05:51
3	have noticed but this report states rather	10:05:56
4	clearly that this device was not finished at all	10:05:59
5	at that time, and we can get to the details. I	10:06:02
6	remember working with Bin Wu B. Wu he's	10:06:05
7	a Chinese person. At that time I believe he was	10:06:11
8	post-doc. I believe also one of Valencia	10:06:13
9	students who were there at the time, I remember	10:06:21
10	we were a group of three people basically working	10:06:26
11	together, but since the other names I don't think	10:06:31
12	were directly involved in this particular case,	10:06:38
13	and we're talking real hard-core engineering	10:06:40
14	development of gates, writing the HDL codes,	10:06:44
15	synthesizing, time enclosure kind of thing.	10:06:52
16	Q. Did you all have strike that.	10:07:03
17	As part of the RD24 project were there	10:07:04
18	regular conference calls or meetings?	10:07:07
19	A. Yes.	10:07:10
20	Q. Did you physically inspect the	10:07:10
21	computer systems that other people in the project	10:07:16
22	were working on?	10:07:19
23	A. Yes, many of them have been set up	10:07:21
24	also for demonstration at CERN. This is one of	10:07:26
25	those sad stories in research, the big labs have	10:07:31

1	the big money, the universities don't, so many of	10:07:35
2	those things were really expensive. So CERN had	10:07:38
3	the money to buy them and then all the	10:07:41
4	universities would basically go to CERN in order	10:07:45
5	to be able to play with them. I used, for	10:07:48
6	example, also the simulation framework developed	10:07:53
7	in Oslo to evaluate and extrapolate performance.	10:07:57
8	I believe the VME system was at CERN.	10:08:03
9	Q. When you say the "VME system",	10:08:08
10	which one are you referring to? The one in	10:08:11
11	Figure 15 or some other one?	10:08:14
12	A. The PCI-SCI card which I focused	10:08:23
13	on is if you look at Figure 4, you will see	10:08:26
14	this device which has a rectangular shape. And	10:08:31
15	it's called PMC 75 by 150 millimeters. "PMC"	10:08:38
16	stands for "PCI mezzanine card". It is not the	10:08:44
17	PCI form factor as set forth in the PCI	10:08:47
18	specification, PCI 2.1, which was the relevant	10:08:51
19	one at that time. There is an add-on spec which	10:08:55
20	says use everything as written in the PCI 2.1	10:09:00
21	spec except for the mechanical form factor, use	10:09:03
22	that form factor and these white connectors to	10:09:06
23	your right, such that you can plug them into	10:09:09
24	a VME board. Most VME processors use PCI also,	10:09:12
25	but in a different form factor because they	10:09:17

1	wouldn't otherwise fit into these crates. And so	10:09:20
2	then, for example now I'm trying to find this	10:09:24
3	picture, it's the VME module with a PMC on it.	10:09:29
4	And these evaluations were done. Yeah, for	10:09:36
5	example, Figure 19 you see the VME board and the	10:09:39
6	PMC card.	10:09:40
7	Q. I see. And you physically saw	10:09:50
8	this? What's shown in Figure 19, is a depiction	10:09:58
9	of something that was built and that you saw at	10:10:02
10	CERN?	10:10:05
11	A. In one or a different	10:10:07
12	incarnations. I mean this is a lab, right?	10:10:09
13	Things have been put together, taken apart,	10:10:12
14	reconnected, yeah, but this system or a variant	10:10:14
15	of that I've certainly seen.	10:10:19
16	Q. And as part of this project, how	10:10:24
17	frequently did you say you travelled to CERN?	10:10:27
18	A. I can't tell exactly, once or	10:10:42
19	twice a year, this kind of thing. You have to	10:10:44
20	remember I was in the U.S. first as a foreigner,	10:10:47
21	I came in on a J-1 visa. Then I changed to	10:10:51
22	an H-1, and then I got the green card based on	10:10:55
23	the national interest waiver. Before I had the	10:10:58
24	green card, leaving the U.S. was quite a painful	10:11:02
25	thing. So this was not just something you just	10:11:03

1	decide and do the next day. But even with this	10:11:06
2	corollary I believe I certainly did one or two	10:11:16
3	trips a year to keep the work going, there is	10:11:19
4	only so much you can do over email and video	10:11:25
5	conferences.	10:11:29
6	Q. In terms of this particular status	10:11:29
7	report, that's Exhibit 1011, do you recall seeing	10:11:31
8	a draft of it before it was submitted?	10:11:38
9	A. I assume so. I don't explicitly	10:11:42
10	recall seeing a draft, this is too long a time	10:11:45
11	ago, but the way this was usually done in	10:11:48
12	fact, in the research field submitting a document	10:11:53
13	with an author on it without the author seeing it	10:11:58
14	beforehand would be an outrage, you can't do that	10:12:01
15	really. But if you ask me, "Do you remember when	10:12:04
16	you saw this?" this I cannot tell, this is too	10:12:07
17	long ago.	10:12:10
18	Q. So standard protocol because your	10:12:10
19	name is on it is that everybody on this	10:12:12
20	particular document would have been provided	10:12:15
21	a copy before it was submitted, correct?	10:12:16
22	A. Good conduct would be and	10:12:19
23	everybody says, "Yes and I agree with the content	10:12:21
24	in there."	10:12:22
25	Q. You say in your declaration that	10:12:24

1	it was submitted to somebody. Who was it	10:12:26
2	submitted to that you recall?	10:12:30
3	A. LHCC Committee. I guess I should	10:12:34
4	do some explanation here	10:12:42
5	Q. Sorry, I apologize but	10:12:42
6	A. LHCC.	10:12:42
7	Q. Okay, so there's also an LHC, what	10:12:42
8	is the difference? What does "LHCC" stand for?	10:12:47
9	Is that the LHC Committee?	10:12:49
10	A. More or less, yes, but I wish to	10:12:52
11	give you a few more details because otherwise	10:12:58
12	this is too broad a term and it doesn't come	10:13:00
13	clear what this is all about.	10:13:02
14	Q. Okay, let me just for clarity ask	10:13:03
15	you what does "LHCC" stand for then?	10:13:06
16	A. This a review committee which was	10:13:08
17	put into place to monitor and evaluate the	10:13:12
18	progress of all related research and development	10:13:17
19	groups of the LHC project and all other projects	10:13:21
20	all together. So, I have reported to the LHCC	10:13:26
21	every three months since 1998 for stuff right	10:13:30
22	outside RD24.	10:13:35
23	This is a very, very tough review	10:13:38
24	process. So you submit a document, you then	10:13:43
25	basically report orally. The committee then	10:13:46

1	writes a report and the report is then reported	10:13:50
2	to the CERN Director and only the committee can	10:13:54
3	defend your project, so you have to teach the	10:13:59
4	reviewers that they defend your project in front	10:14:02
5	of the CERN Director, Scientific Director.	10:14:05
6	So the idea behind it is that you have	10:14:08
7	to be it's not just, you know, you thumb over	10:14:10
8	some documents and say, "Well it's cool, it's all	10:14:13
9	right", but a very stringent, very tough review	10:14:16
10	process in order to make sure that this huge	10:14:20
11	highly complex project has a chance of	10:14:23
12	succeeding.	10:14:25
13	All these processes were following a	10:14:27
14	rather strict order and an internal rule set.	10:14:31
15	The reviewers were usually set out to accompany	10:14:37
16	a particular project for a longer period of time,	10:14:40
17	we're talking several years, and if the reviewers	10:14:43
18	would say, "This project is not performing"	10:14:49
19	rather tough scrutiny would happen. I've seen it	10:14:53
20	happening fortunately never in my own case	10:14:57
21	that you get down to weekly and even daily	10:15:00
22	reports when you're really starting to get into	10:15:04
23	bad shape.	10:15:08
24	The idea behind it is to have a complete	10:15:09
25	view of this huge development the same was	10:15:11

1	done for the accelerator, for example to make	10:15:14
2	sure that everything comes together in time.	10:15:16
3	Q. So I understand it, there are	10:15:18
4	a number of different projects that were related	10:15:21
5	to the LHC and this RD24 was one of those	10:15:23
6	projects, correct?	10:15:30
7	A. Yes.	10:15:31
8	Q. And so the status report was	10:15:31
9	a report created by the RD24 working group that	10:15:33
10	was submitted to the LHCC as part of some	10:15:38
11	periodic review?	10:15:42
12	A. Yeah.	10:15:43
13	Q. Okay. Who is on the LHCC at that	10:15:44
14	time? In general, what kinds of people?	10:15:47
15	A. People my status.	10:15:52
16	Q. Okay.	10:15:53
17	A. Director of an institute, full	10:15:54
18	professor, ten years' minimum experience in the	10:15:59
19	field, highly outstanding scientific record,	10:16:01
20	publication record. And, in fact, it was	10:16:08
21	an issue over time because this is a huge	10:16:10
22	amount of work for the reviewers, too to	10:16:12
23	really find people at that level. We're talking	10:16:15
24	around the globe, all time zones, they all had to	10:16:17
25	travel to CERN, get together, do their work.	10:16:23

1	Such a review, the bigger ones which were	10:16:25
2	quarterly, usually took a couple of days	10:16:29
3	depending on the size of the project. Now, RD24	10:16:31
4	would be considered a small project, right? If	10:16:34
5	you take the ALICE experiment, the ALICE	10:16:37
6	experiment had some 20 subprojects, where each	10:16:40
7	one was at least at large as RD24 and they all	10:16:44
8	were reviewed like that, you know.	10:16:47
9	Q. So, how many people in this	10:16:49
10	1996-1998 timeframe sat on the LHCC?	10:16:54
11	A. I can't give you an exact number.	10:17:01
12	We're talking a handful, three, four, five.	10:17:03
13	Depending on the particular project being	10:17:07
14	reviewed. In the case of ALICE the group was	10:17:11
15	larger because the spread of different	10:17:16
16	technologies was larger. Here this is in	10:17:18
17	quotes only computer architecture, computer	10:17:24
18	engineering. Normally you have detector physics	10:17:27
19	on top of it, material science. Detectors are	10:17:31
20	highly complex devices pushing the limits of	10:17:35
21	material science, for example, so you have people	10:17:38
22	understanding that also.	10:17:40
23	But the LHCC is a whole body all	10:17:42
24	together, so it would all come together then and	10:17:45
25	then be reported, all subprojects. It's a big	10:17:48

1	thing.	10:17:51
2	Q. So at the top of the document	10:17:52
3	there's a heading in the right and it says:	10:17:57
4	"CERN/LHCC" and then "LHCC 96-33". Do	10:18:01
5	you know what that means?	10:18:10
6	A. I would assume this is the year	10:18:13
7	and probably the 33rd kind of meeting of that.	10:18:15
8	The exact number scheme I don't know. It's	10:18:19
9	an internal LHCC coding so that they find their	10:18:24
10	reports.	10:18:27
11	Q. Okay, and then it says "LCB Status	10:18:27
12	Report". Do you know what "LCB" means?	10:18:32
13	A. I do, but now I don't remember the	10:18:37
14	exact acronym. It could be LHC Computing Board,	10:18:41
15	something like that.	10:18:49
16	Q. And the "2 October 1996", you	10:18:53
17	indicate in your declaration that you believe	10:18:58
18	that is the date that this status report was	10:19:00
19	submitted to the LHCC; is that correct?	10:19:02
20	A. Yeah.	10:19:05
21	Q. And what is the basis for do	10:19:05
22	you have any basis for that other than your	10:19:12
23	memory for saying that that's the date it was	10:19:15
24	submitted to the committee?	10:19:17
25	A. This is a status report of	10:19:20

1	a working group which is basically documenting	10:19:22
2	a work in progress. Many things in here are	10:19:28
3	outlined as options for the future or how one	10:19:33
4	could do things, what are the things which are	10:19:36
5	essential to be built, how far the process of	10:19:41
6	building has come. And obviously that has to	10:19:43
7	have a date as of when this status has been	10:19:46
8	written and submitted because obviously if you	10:19:49
9	report time in progress, the next day it's	10:19:52
10	already invalid, strictly spoken, and this is the	10:19:54
11	date when this was submitted. There is no other	10:19:57
12	date on this document.	10:20:00
13	Q. Right so	10:20:01
14	A. I have one question or favor to	10:20:01
15	ask. I would like to go to the bathroom.	10:20:05
16	MR. BUROKER: Oh, yeah, I should have	10:20:08
17	said at the beginning, any time you need to take	10:20:09
18	a break, we can take a break. So let's go off	10:20:11
19	the record and take a short break.	10:20:14
20	(Brief recess 10:20 a.m 10:27 a.m.)	10:27:41
21	BY MR. BUROKER:	10:27:45
22	Q. Sir, looking at paragraph 170 of	10:27:48
23	the declaration we were looking at before in the	10:27:53
24	'814 proceeding, you state that the date on the	10:28:00
25	front of the Bogart reference, which is	10:28:03

1	Exhibit 1011 we were looking at, has a date and	10:28:05
2	that's the date submitted to the CERN LHCC	10:28:09
3	Committee. That's your testimony, correct?	10:28:14
4	A. Yeah.	10:28:15
5	Q. And you don't cite anything to	10:28:16
6	support that, that's just your testimony based on	10:28:19
7	your memory of how the proceedings were, correct?	10:28:25
8	MR. DAVIS: Objection; form.	10:28:31
9	BY MR. BUROKER:	10:28:32
10	Q. Right? Next to that sentence	10:28:33
11	there's no citation to any other document or	10:28:34
12	piece of evidence, just your memory, correct?	10:28:36
13	A. Well, I mean if you write	10:28:39
14	a document, a report of any sort, in particular	10:28:41
15	a status report, it is completely invalid without	10:28:46
16	a date. So this date has to be the date when	10:28:49
17	this report was finalized as the status of the	10:28:59
18	RD24 project at that time. If you would remove	10:29:04
19	that date, or declare it to be something else,	10:29:12
20	this status report would be meaningless.	10:29:15
21	Q. Right. But you're trying	10:29:17
22	strike that.	10:29:17
23	You're saying also that that date	10:29:23
24	represents the date submitted to committee and	10:29:25
25	not the date of its public availability or	10:29:28

1	indexing by the library. And for that	10:29:31
2	proposition you also do not cite anything,	10:29:36
3	correct?	10:29:38
4	MR. DAVIS: Objection; form.	10:29:39
5	THE WITNESS: This is the date which	10:29:43
6	defines the status of that report and this is the	10:29:51
7	date when it was submitted this is the date	10:29:53
8	when it was given to the LHCC, possibly one or	10:29:58
9	two days later. Usually they were written up to	10:30:02
10	the last minute, you know, all these reports are	10:30:04
11	usually generated, everybody's late. And from	10:30:07
12	this document, or anything I've seen so far, I	10:30:13
13	have not seen any evidence that says that it was	10:30:19
14	then publicly available, that's correct.	10:30:23
15	BY MR. BUROKER:	10:30:25
16	Q. All right. But you also don't	10:30:25
17	know, and can't provide testimony, that it wasn't	10:30:28
18	publicly available as of October 2, 1996, right?	10:30:32
19	MR. DAVIS: Objection; form.	10:30:37
20	THE WITNESS: I mean here I wish really	10:30:41
21	to stick to what I say in my report. What do we	10:30:47
22	have here? I'm saying I'm unaware of any day	10:30:52
23	prior to the priority filing date of the '814	10:30:59
24	Patent that the RD24 report was published,	10:31:03
25	indexed or made available to the public, which	10:31:05

1	are the relevant things here. So this is what it	10:31:07
2	is: I'm not aware. I'm not saying it was, I'm	10:31:13
3	not saying it was not, I'm just not aware.	10:31:17
4	BY MR. BUROKER:	10:31:20
5	Q. Okay. In the previous sentence,	10:31:21
6	you say strike that. Let me come back to	10:31:22
7	that.	10:31:28
8	Then in paragraph 171 you make reference	10:31:29
9	to:	10:31:37
10	" bibliographic data on the CERN	10:31:43
11	library server that lists the Bogaerts reference	10:31:46
12	as 'submitted by October 2, 1996'"	10:31:50
13	And you say:	10:31:52
14	"[It] relates to the date the	10:31:52
15	report was submitted to the committee; it	10:31:53
16	does not relate to the day the RD24 report was	10:31:55
17	available or indexed in the CERN library."	10:31:59
18	What's your basis for saying that?	10:32:02
19	A. Is there any date? I can't see	10:32:05
20	any date on the CERN library stamp. I mean this	10:32:08
21	is an index basically uniquely identifying this	10:32:11
22	document as part of the CERN library, it says	10:32:14
23	nothing about its public availability. And one	10:32:17
24	should make one thing perfectly clear here, even	10:32:21
25	if a document is in the CERN library, it's far	10:32:24

1	from being publicly available. In order to get	10:32:26
2	to the CERN library you have to cross the CERN	10:32:29
3	entry, and the CERN entry you can only cross if	10:32:32
4	you're a CERN member. The United States are not	10:32:34
5	member state of CERN. So, for instance, nobody	10:32:38
6	from the U.S. could easily be entering CERN at	10:32:41
7	all. You first have to become at least a guest	10:32:45
8	of CERN, which means you have to have a project	10:32:49
9	at CERN or with high relevance to CERN, like I	10:32:52
10	did, but I had my ID already beforehand, and then	10:32:56
11	you can go to the CERN library on site of CERN.	10:32:59
12	Be aware, CERN is an international organization;	10:33:03
13	when you enter CERN you basically leave	10:33:06
14	Switzerland, right? It is a state in itself, and	10:33:09
15	has very high standards with respect to its	10:33:13
16	autonomy. So even if this document is in the	10:33:15
17	CERN library, it doesn't say that it	10:33:20
18	automatically is on the internet. There is	10:33:24
19	a huge amount of documents in the CERN library	10:33:26
20	which would also never make it to the internet	10:33:27
21	because of all the copyright issues associated.	10:33:30
22	Q. But a document doesn't have to be	10:33:38
23	on the internet to be a publication under U.S.	10:33:40
24	patent law, correct?	10:33:45
25	A. Right. Now, if you're referring	10:33:46

1	to the there is a definition for public	10:33:49
2	availability which I have put in here I believe.	10:33:53
3	Do you want me to cite it?	10:33:58
4	Q. Well, if you need to to answer the	10:33:59
5	question I asked which is that a document doesn't	10:34:02
6	have to be on the internet to be considered	10:34:05
7	a publication under U.S. patent law?	10:34:07
8	MR. DAVIS: Objection; form.	10:34:10
9	THE WITNESS: Let me just pull this out	10:34:14
10	to be really precise. (The witness reviewed the	10:34:15
11	document.)	10:34:15
12	Right:	10:34:27
13	"A reference must have been made,	10:34:27
14	known, used, sold, offered for sale, published,	10:34:30
15	or patented or be the subject of a patent	10:34:32
16	application by another, before the priority date	10:34:34
17	of the patent."	10:34:36
18	There is also a section which says the	10:34:37
19	index is searchable so that it can be found.	10:34:40
20	That section I have a problem finding at this	10:34:49
21	moment. Ah, here we are, page 8, paragraph 19:	10:34:52
22	"I understand that a reference is	10:35:00
23	considered publicly accessible if it was	10:35:01
24	publicly disseminated or (2) otherwise made	10:35:04
25	available to the extent that persons interested	10:35:08

1	and ordinarily skilled in the subject matter or	10:35:12
2	art, exercising reasonable diligence, could	10:35:14
3	locate it."	10:35:17
4	And, I mean, this is the sentence here,	10:35:20
5	right? Because it was stored in a library	10:35:22
6	doesn't mean it's publicly available and this is	10:35:25
7	why I made this statement about the CERN library.	10:35:29
8	BY MR. BUROKER:	10:35:31
9	Q. Well the next sentence though you	10:35:31
10	say you recognize that if it's in a library and	10:35:33
11	it's indexed and cataloged by title or subject	10:35:35
12	matter that's a factor that means it could be	10:35:38
13	considered publicly accessible?	10:35:41
14	A. Provided the library has public	10:35:44
15	access. If there is a library which is private,	10:35:46
16	you can't get to, and there is no public access.	10:35:48
17	Q. Well that's not what it says in	10:35:51
18	your declaration; you didn't say that the library	10:35:53
19	has to be publicly accessible.	10:35:55
20	MR. DAVIS: Objection; form.	10:35:58
21	BY MR. BUROKER:	10:35:59
22	Q. Did you?	10:36:00
23	A. Can you where did I say that?	10:36:07
24	Q. Well that's my point. I don't	10:36:08
25	believe you said the last part of your answer	10:36:10

1	in the previous question was "provided the	10:36:11
2	library has public access". I don't think that	10:36:14
3	any of this text in paragraph 19 says that the	10:36:16
4	library has to have public be accessible to	10:36:18
5	the public, does it?	10:36:22
6	MR. DAVIS: Objection; form.	10:36:24
7	THE WITNESS: Well, take paragraph 19,	10:36:30
8	second sentence:	10:36:32
9	"I understand that publicly accessible	10:36:32
10	requires that a reference must have been	10:36:36
11	sufficiently accessible to the public interested	10:36:38
12	in the art."	10:36:41
13	BY MR. BUROKER:	10:36:43
14	Q. Right, and one of the kinds of	10:36:44
15	people who would be interested in the art would	10:36:45
16	have been a person working on computer	10:36:47
17	architecture as part of some of the CERN	10:36:52
18	projects, right?	10:36:56
19	MR. DAVIS: Objection; form.	10:36:56
20	THE WITNESS: Not necessarily.	10:36:57
21	BY MR. BUROKER:	10:37:00
22	Q. Were you interested in the art?	10:37:01
23	A. Yes.	10:37:03
24	Q. And you could have accessed it,	10:37:03
25	correct?	10:37:04

1	A. I have a very particular history	10:37:04
2	in this particular field, but this field is of	10:37:07
3	course much broader and larger than just nuclear	10:37:15
4	physics.	10:37:19
5	Q. Well, anybody on this RD24 status	10:37:19
6	report, any of these people would have had access	10:37:21
7	to the CERN library in 1996, correct?	10:37:23
8	A. Absolutely, yes.	10:37:25
9	Q. Among other people working on	10:37:26
10	various LHC projects?	10:37:28
11	A. Correct. Basically all CERN	10:37:31
12	users.	10:37:38
13	Q. You agree that this document was	10:37:40
14	at some point provided to the CERN library,	10:37:45
15	right?	10:37:48
16	A. Correct. Otherwise there wouldn't	10:37:50
17	be the library stamp on it.	10:37:51
18	Q. Okay. Do you have any knowledge	10:37:53
19	regarding the procedure by which this document	10:38:01
20	was provided to the CERN library?	10:38:04
21	A. I would assume it's the normal	10:38:08
22	procedure, submission to the library, library	10:38:10
23	records it, puts the stamp on it. Other than	10:38:14
24	that no, and I was not involved when this	10:38:17
25	happened.	10:38:20

1	Q. Did you ask Dr. Müller if he	10:38:20
2	submitted it to the library?	10:38:27
3	A. I asked him whether he had	10:38:28
4	a recollection when it was done and he said no.	10:38:30
5	I didn't ask him explicitly, "Did you do this?"	10:38:32
6	but I believe that one can assume that he did.	10:38:35
7	Q. So it's possible that he submitted	10:38:39
8	it to the library at the same time that he	10:38:40
9	submitted it to the CERN LHCC Committee, correct?	10:38:43
10	A. I don't know that.	10:38:49
11	Q. It's possible and also not	10:38:51
12	possible, right?	10:38:54
13	MR. DAVIS: Objection; form.	10:38:59
14	THE WITNESS: I mean, in general, keep	10:39:00
15	in mind the frame setting of this here, this is	10:39:02
16	a tough review committee, you're reporting to	10:39:06
17	such a review committee. I would never, ever	10:39:09
18	submit an internal document I give to a reviewer,	10:39:14
19	in particular if it contains some confidential	10:39:18
20	information, at the same time to the library. It	10:39:20
21	doesn't seem to be the this is not the right	10:39:29
22	process. I mean it goes to the review committee,	10:39:31
23	there are reports written about that and if	10:39:33
24	anything, at some point, the whole package with	10:39:35
25	recommendations of the reviewers and so forth	10:39:40

1	would possibly make it then to the library as	10:39:43
2	a final result of a complete process.	10:39:46
3	Now, since this process was an ongoing	10:39:49
4	thing, prior to the review I would have certainly	10:39:52
5	not expected anybody to submit something to the	10:39:56
6	library. It may also be that the LHC Committee	10:39:58
7	at some point later, for instance at the	10:40:02
8	conclusion of the RD24 project, took the whole	10:40:05
9	package and submitted it to the library. I don't	10:40:09
10	know the exact process that happened here.	10:40:11
11	BY MR. BUROKER:	10:40:15
12	Q. Do you have any expertise or	10:40:15
13	knowledge about CERN library's procedures?	10:40:18
14	A. Not in depth. I'm using the	10:40:21
15	library of course, but we submit our documents to	10:40:23
16	our own libraries, but the procedures how	10:40:30
17	libraries work are relatively simple.	10:40:35
18	Q. Do you know whether the CERN	10:40:37
19	library, as part of its normal practice back in	10:40:38
20	1996, would receive copies of everything sent to	10:40:41
21	the HCCC (sic)?	10:40:44
22	MR. DAVIS: Objection; form.	10:40:48
23	BY MR. BUROKER:	10:40:50
24	Q. Excuse me to the LHCC. I used the	10:40:50
25	wrong acronym.	10:40:53

1	MR. DAVIS: Objection; form.	10:40:55
2	THE WITNESS: I would doubt that since	10:41:00
3	you said "everything".	10:41:01
4	BY MR. BUROKER:	10:41:02
5	Q. Do you know whether, as part of	10:41:02
6	the normal procedures, the LHCC would provide	10:41:05
7	copies of status reports to the library?	10:41:10
8	A. I'm not aware that all my status	10:41:21
9	reports and I wrote a lot of them for my	10:41:23
10	own projects I had later for the LHC project were	10:41:25
11	all submitted to the library, I'm not aware of	10:41:31
12	that. Now, I haven't though done an in-depth	10:41:33
13	search, but I would find it highly unusual and	10:41:37
14	inappropriate in particular since I wasn't asked.	10:41:42
15	Q. Is there a physical library still	10:41:44
16	at CERN?	10:41:49
17	A. Oh yes.	10:41:50
18	Q. And so you visited the library	10:41:50
19	during the '96 to '98 timeframe?	10:41:53
20	A. Yeah, from time to time, it's	10:41:57
21	pretty big.	10:41:58
22	Q. And at that time was there also a	10:41:59
23	network-based access to the library's database,	10:42:04
24	so that if somebody were looking to see what was	10:42:08
25	available and you were in California, for	10:42:10

1	example, could you link in to find out what was	10:42:12
2	there?	10:42:15
3	A. I never did that from California,	10:42:16
4	certainly not when at CERN. I went there.	10:42:18
5	Whether they had an electronic index already at	10:42:22
6	that time I'm not sure, I don't remember. I	10:42:25
7	still remember they have even these huge rows,	10:42:28
8	where you have all these little library cards,	10:42:33
9	with the index and so forth as it used to be.	10:42:38
10	Q. Did you attempt to contact anyone	10:42:45
11	with a CERN library connection with trying to	10:42:48
12	determine whether or not this Bogaerts reference	10:42:51
13	was	10:42:57
14	A. I did not.	10:42:57
15	Q publicly available?	10:42:58
16	Have you submitted documents to the CERN	10:43:00
17	library in the past?	10:43:04
18	A. Directly, no. And this is highly	10:43:08
19	unusual, wouldn't do that. The way it works is	10:43:11
20	the CERN library is a library usually doesn't	10:43:19
21	accept ordinary work in progress or status report	10:43:25
22	material. The library usually wants finalized	10:43:29
23	documents: a thesis, an approved paper. There is	10:43:33
24	this area of grey literature, which is what we	10:43:39
25	call preprints, almost the proof paper, so papers	10:43:41

1	submitted for acceptance. CERN has a rather	10:43:44
2	complex way of accepting publications so, unlike	10:43:49
3	in other areas where we have this rule of freedom	10:43:54
4	to publish anything you want, at CERN you can't	10:43:59
5	do that. If I wish to write a paper in the	10:44:03
6	context of a CERN experiment it has to be	10:44:05
7	submitted first to the committee inside CERN, the	10:44:07
8	committee will review that, we're talking	10:44:09
9	something like ten people typically on such	10:44:11
LO	a committee. The paper is being iterated many,	10:44:13
11	many times, it can take half a year, sometimes	10:44:19
12	a year before it's approved. Once it's approved	10:44:22
L3	it's submitted for publication with a CERN	10:44:24
L 4	approval, and once the paper is accepted for	10:44:29
L5	publication then by the book or magazine, whoever	10:44:33
L 6	publishes, Phys Ref Letters and so forth, then it	10:44:39
L7	would make its way into the library and that,	10:44:44
L8	again, only under certain conditions because	10:44:46
L 9	there are publishing agencies which forbid that	10:44:49
20	and then you find in the library only a reference	10:44:52
21	saying if you want a copy of that document you	10:44:55
22	have to either go to the publishing house. In	10:44:57
23	case of Phys Ref Letters CERN of course has	10:45:02
24	bought a license to that magazine.	10:45:09
25	O. Wait, are you saving "list of	10:45:10

1	letters"? What are you saying?	10:45:11
2	A. Physical Review Letters.	10:45:14
3	Q. Okay, I apologize. She's not	10:45:15
4	getting it and we want a clear record.	10:45:17
5	A. That's fine, Phys Ref Letters is	10:45:20
6	the short form. I apologize for that. They are	10:45:25
7	always cited as that and this is	10:45:28
8	Q. Phys Ref, okay, I got you.	10:45:28
9	A. Yeah. Because they have very high	10:45:29
10	impact points, and this is, in physics, very	10:45:32
11	important to have a publication in Phys Ref.	10:45:34
12	But, for example, if you publish it in certain	10:45:38
13	magazines, they do not allow you to use it	10:45:43
14	anywhere else, you also have to buy then the	10:45:47
15	magazine and that means for this particular	10:45:50
16	magazine there is no electronic version, you have	10:45:52
17	to go to the CERN library and pull the physical	10:45:55
18	paper out of the shelf to be able to read it and	10:45:58
19	make copies and so forth.	10:46:03
20	There is a long and ongoing debate, not	10:46:04
21	settled, about all of this, because it turns out	10:46:07
22	that the electronic version of a paper often is	10:46:13
23	more expensive than just buying the paper version	10:46:16
24	of a magazine, but the paper version is highly	10:46:18
25	inconvenient because, you know, it takes a lot of	10:46:22

1	time before you have it and so forth. But the	10:46:24
2	fact is, if all these conditions are met, a paper	10:46:29
3	approved for publication is out there, it is real	10:46:32
4	and the paper is part of the stuff the library	10:46:36
5	buys anyway. I mean Phys Ref Letters costs	10:46:41
6	something like 30 or 40,000 a year if I remember	10:46:45
7	correctly, really expensive. Then you can have	10:46:47
8	it in the library. It's not yet on the internet;	10:46:49
9	only if CERN also acquired an internet license	10:46:54
10	for that magazine and it is also available.	10:46:58
11	So, you see, this is absolutely a	10:47:00
12	non-trivial thing and libraries have to be	10:47:03
13	really, really careful. Imagine even just one	10:47:06
14	version of a copyrighted paper ends up on the	10:47:09
15	internet without approval, you immediately have	10:47:13
16	all the litigation for damages and so forth.	10:47:15
17	Q. So I think that the question was	10:47:20
18	whether you had ever submitted the document to	10:47:23
19	CERN for publication and the answer was no,	10:47:26
20	right?	10:47:30
21	A. I would submit it to the	10:47:30
22	committee, the committee would publish it and	10:47:31
23	then, as part of the automatic process, it would	10:47:33
24	eventually end up in the library. So, strictly	10:47:36
25	spoken, directly? No. Indirectly according to	10:47:39

1	the procedure set forth? Yes.	10:47:42
2	Q. So some documents that you've	10:47:44
3	submitted to committee have been published or are	10:47:47
4	part of the publications of the CERN library but	10:47:53
5	through the committee process; is that right?	10:47:55
6	A. Yeah.	10:47:57
7	MR. DAVIS: Objection; form.	10:47:57
8	BY MR. BUROKER:	10:47:57
9	Q. And that's the same committee, the	10:48:00
10	LHCC Committee or is there a different Committee	10:48:02
11	you're referring to?	10:48:04
12	A. No, no, no totally different. The	10:48:04
13	LHCC Committee is only there to monitor the	10:48:06
14	process of development work for LHC-related	10:48:08
15	experiments or accelerator, okay? Now we have	10:48:13
16	LHC in operation since a couple of years and	10:48:23
17	experiments are taking data and analyzing data.	10:48:31
18	So, for instance, I'm a member of the ALICE	10:48:33
19	Collaboration. This is 1,100 scientists. So	10:48:36
20	a publication like this one, has a two- or	10:48:39
21	three-page front page stating all the times	10:48:43
22	right, 1,000 names is a lot of stuff with all	10:48:45
23	the affiliations, and inside ALICE we have	10:48:49
24	a Publication Committee which has at least five	10:48:56
25	or six subgroups focusing at different subfields	10:49:01

1	of the physics which ALICE does. And every	10:49:04
2	single paper goes through that process. There is	10:49:08
3	even a mitigation framework there. So, for	10:49:13
4	example, if the author doesn't agree with what	10:49:17
5	the committee wants changed, then it's escalated,	10:49:19
6	worst case, to the ALICE Management Board and	10:49:22
7	a decision is being made and so forth. But this	10:49:25
8	is now a scrutiny process which is inside ALICE.	10:49:28
9	On top of that it's really highly complicated.	10:49:33
10	If you have what is considered	10:49:38
11	a discovery-level publication, you found a new	10:49:42
12	particle, even then ALICE cannot publish it.	10:49:44
13	Then it goes to the CERN Director and the CERN	10:49:48
14	Director will put a hold on that paper until he's	10:49:52
15	convinced that (a) it is absolutely solid and	10:49:55
16	correct and (b) if there is the possibility of	10:50:00
17	a second CERN experiment measuring it he likes to	10:50:03
18	see them measuring it, too, to have a second	10:50:06
19	validation. You may remember the cold fusion	10:50:09
20	case which happened in Germany and somebody made	10:50:12
21	huge noise, big press media, about having found a	10:50:16
22	way to do fusion basically in the laboratory and	10:50:22
23	that was a hoax; big embarrassment for everybody.	10:50:26
24	So CERN has put a very, very high level of	10:50:30
25	scrutiny to avoid this from happening and yet you	10:50:35

1	may have noticed the big press campaign about	10:50:38
2	CERN having measured a particle traveling faster	10:50:40
3	than the speed of light, which was wrong and yet	10:50:42
4	it went out. So even there the scrutiny failed.	10:50:46
5	Q. So I'm going to ask you to listen	10:50:54
6	to my questions and answer those questions. I	10:50:55
7	know you like to go on and explain your answers,	10:50:58
8	and I mean your counsel can ask you follow-up	10:51:01
9	questions if he needs to. My question was: was	10:51:03
10	it a different committee?	10:51:07
11	A. Yes.	10:51:08
12	Q. Thank you. In the 1996 timeframe,	10:51:08
13	when the Exhibit 1011 was submitted, do you know	10:51:21
14	what the procedure was for LHCC to submit	10:51:27
15	a document to the library? If there is such	10:51:35
16	a procedure?	10:51:38
17	MR. DAVIS: Objection; form.	10:51:39
18	THE WITNESS: No explicit set of rules	10:51:45
19	comes to my mind, except that it's the same	10:51:49
20	standard procedure how libraries worked. No	10:51:53
21	particular rules I remember.	10:51:56
22	BY MR. BUROKER:	10:52:02
23	Q. Do you recall personally	10:52:02
24	submitting this report to anyone after it was	10:52:05
25	submitted to the LHCC?	10:52:11

1	A. No.	10:52:13
2	Q. Do you know whether Dr. Müller	10:52:14
3	submitted this document to anyone other than the	10:52:18
4	LHCC at that time in 1996?	10:52:22
5	A. No, and I was surprised because	10:52:26
6	there were quite a few confidentiality agreements	10:52:28
7	associated with this.	10:52:31
8	Q. Right. So you do give some	10:52:37
9	testimony in your declaration about	10:52:39
10	confidentiality.	10:52:42
11	Paragraph 170, for example, of the '814	10:52:47
12	declaration says that:	10:52:54
13	" it is likely that the RD24 status	10:52:59
14	report would NOT have been published on that date	10:53:01
15	because it was subject to confidentiality	10:53:04
16	agreements."	10:53:06
17	A. That's correct.	10:53:06
18	Q. You don't cite to what those	10:53:07
19	confidentiality agreements are in this	10:53:12
20	declaration, correct?	10:53:15
21	A. Yes, correct.	10:53:16
22	Q. And the document itself doesn't	10:53:17
23	have any confidentiality labels that I've been	10:53:21
24	able to find. Have you been able to find any?	10:53:24
25	A. I did not, no. Although I didn't	10:53:27

1	explicitly look for them but no.	10:53:31
2	Q. And you agree that, as of 2014 at	10:53:58
3	least, or 2015, this document is now publicly	10:54:04
4	accessible, correct?	10:54:09
5	MR. DAVIS: Objection; form.	10:54:12
6	THE WITNESS: The big question is now	10:54:16
7	what do you mean with "this document"? If you	10:54:18
8	mean the version with the CERN library stamp as	10:54:20
9	it was then, yes, one can find it now through the	10:54:24
10	internet on the CERN library pages. I Googled	10:54:35
11	for it and I did find it, yes.	10:54:40
12	BY MR. BUROKER:	10:54:43
13	Q. Okay. And you don't have any	10:54:43
14	information about when between 1996 and 2014 this	10:54:44
15	did become publicly available, correct?	10:54:54
16	A. Correct, I cannot tell you the	10:54:56
17	date.	10:54:57
18	Q. And Dr. Müller couldn't tell you	10:54:59
19	the date, correct?	10:55:02
20	A. No. Yeah, correct. Yes, I should	
21		10:55:03
	say something here. You've just asked a negative	10:55:07
22	question, right? "Could not".	10:55:12
23	Q. Yeah, and if you want to	10:55:14
24	A. No, no, to make it clear, I tried	10:55:16
25	to be very correct here and there is a little but	10:55:19

1	nasty pitfall; the correct answer to a negative	10:55:23
2	question in the U.S. is "no". The affirmative	10:55:28
3	answer to a negative question is "no" is	10:55:31
4	"yes", sorry, in Germany it is "no".	10:55:35
5	Q. Okay, let me ask it again.	10:55:37
6	Did Dr. Müller know when this document	10:55:39
7	became publicly available?	10:55:45
8	A. He could not tell, arguing, "This	10:55:46
9	is almost 20 years ago, how would I know? This	10:55:49
10	is more than 20 years ago when I wrote this, how	10:55:53
11	would I know?"	10:55:56
12	Q. There's some discussion in the	10:56:14
13	declaration about I guess it starts on	10:56:15
14	paragraph 174 about the internet linking of	10:56:18
15	this report, or a copy of this report. So I want	10:56:25
16	to ask you some questions about that.	10:56:32
17	You say in your declaration at	10:56:35
18	paragraph 176 that you believe:	10:56:38
19	" that the RD24 status report	10:56:42
20	was	10:56:42
21	which is the Bogaerts reference, and	10:56:46
22	let me find the right language:	10:56:50
23	" inadvertently linked to a public	10:56:52
24	web page on Mr. Müller's private web server and	10:56:55
25	was later removed."	10:56:58

1	Do you see that at the end of 176?	10:56:59
2	A. Yes.	10:57:05
3	Q. Did you discuss this piece of	10:57:14
4	information with Mr. Müller?	10:57:16
5	A. No.	10:57:17
6	Q. You didn't ask him?	10:57:18
7	A. I did not. I didn't see any point	10:57:19
8	because no, I didn't ask, no.	10:57:22
9	Q. What is the basis for your	10:57:27
10	statement that you believe it was "inadvertently	10:57:29
11	linked"?	10:57:33
12	A. The machine sunshine is one of the	10:57:37
13	machines that Hans Müller used at that time.	10:57:44
14	Although it's long ago I still remember that	10:57:50
15	because it was these nice shiny flat boxes and	10:57:52
16	quite expensive, I wanted one, too, but at first	10:57:57
17	I didn't have one, so these are the things you	10:57:59
18	remember. And since it's the machine built by	10:58:01
19	Sun MicroSystems he called them sunshine and the	10:58:06
20	other one was called sunrise, being the machines	10:58:09
21	of the RD24 project basically his personal	10:58:13
22	machines he used to work with.	10:58:17
23	And you see that the URL specified here	10:58:18
24	has this ":8080" after it. This is the URL or	10:58:30
25	HTTP syntax which specifies the port number. The	10:58:38

1	port number is a number used in the internet to	10:58:41
2	identify a particular sub-functionality of	10:58:45
3	a computer. The official port number for	10:58:48
4	internet web access the World Wide Web is	10:58:51
5	port 80. Most of the computers at the time came	10:58:54
6	already with a private web server built in, used	10:58:58
7	for all sorts of maintenance functionality and so	10:59:01
8	forth. And usually if you just wanted to set up	10:59:05
9	something for your own contacts and work you	10:59:09
10	might use a different port number and Hans Müller	10:59:13
11	invented 8080. Obviously it is clear where it	10:59:17
12	comes from. This number has to be between one	10:59:19
13	and 65,535, so you have roughly 65,000 options.	10:59:22
14	However, the internet search engines usually use	10:59:32
15	the internet addresses, so port 80, right? So if	10:59:38
16	you typed www.ibm.com, you'd definitely end up at	10:59:42
17	a port of 80. So, from that point of view	10:59:49
18	an ordinary search engine and one should know	10:59:57
19	at that time there were not that many search	11:00:00
20	engines, I'm not sure Google already existed at	11:00:03
21	all that would look for any other port. And	11:00:08
22	it would not be successful if you were to try to	11:00:11
23	just screen whether or not a computer is using	11:00:14
24	another port because that would be detected by	11:00:17
25	the computer security infrastructure and you	11:00:21

1	would be considered a hacker and you would be	11:00:23
2	blocked completely. CERN does that completely	11:00:27
3	automatically.	11:00:29
4	So for this document to be found there	11:00:32
5	must have been by any web crawler, as these	11:00:34
6	machines are being called, you know, which go on	11:00:40
7	websites, try to read everything, store it	11:00:43
8	somewhere and then follow links, the only	11:00:47
9	reasonable way for this to be done, would be that	11:00:49
10	some link somewhere would have redirected to this	11:00:53
11	point. This is the rationale behind that	11:00:58
12	statement.	11:01:00
13	Q. Okay, but the fact of the matter	11:01:00
14	is it was linked and captured by the internet	11:01:02
15	archive in 1996, right?	11:01:07
16	A. That document was submitted, yes,	11:01:10
17	although this is, if I remember correctly, only	11:01:13
18	part of it some different pages, but they have	11:01:16
19	certain fraction of it, yes.	11:01:19
20	Q. Well, they have a postscript	11:01:24
21	file that if you click on it you get the entire	11:01:26
22	document, correct? Did you try it?	11:01:29
23	MR. DAVIS: Objection; form.	11:01:30
24	BY MR. BUROKER:	11:01:32
25	Q. Did you personally visit this U	11:01:32

1	looking in paragraph 174, there's a URL, there's	11:01:37
2	two URLs. The top one excuse me, the second	11:01:47
3	one is a postscript file, correct?	11:01:52
4	A. The second?	11:01:55
5	MR. DAVIS: Objection; form.	11:01:56
6	BY MR. BUROKER:	11:01:59
7	Q. The second link?	11:01:59
8	A. So the second link and you're	11:02:00
9	referring to the HTTP "web.archive/web" and	11:02:03
10	then all sorts of long numbers,	11:02:07
11	"sunshine.cern.ch:8080RD2496_1.ps". Yeah, the	11:02:10
12	extension ".ps" indicates it's be to a postscript	11:02:17
13	file.	11:02:20
14	Q. Right. And did you visit that	11:02:20
15	URL?	11:02:23
16	A. I'm not sure.	11:02:24
17	Q. And did you visit that URL and	11:02:27
18	click on that link and see what response you got	11:02:32
19	back?	11:02:34
20	A. I can't tell you. I did click on	11:02:38
21	a few of those references but for this particular	11:02:42
22	one I can't tell you.	11:02:48
23	Q. And a postscript file is an Adobe	11:02:49
24	file format that builds a PDF, correct?	11:02:54
25	A. No.	11:02:58

1	Q. What is a postscript file?	11:02:58
2	A. At the time we're discussing here,	11:03:07
3	1996, PDF did not exist. Postscript is a page	11:03:09
4	description language, which was invented by Adobe	11:03:13
5	also, which basically has all elements to	11:03:16
6	basically print any kind of document, any form,	11:03:22
7	any kind of graphics, whatsoever. It's a page	11:03:26
8	description language in the strictest sense, it	11:03:33
9	has commands in there, certain rules. So, for	11:03:36
10	example, if you have a text and it has to be	11:03:41
11	modified then there are commands saying make this	11:03:42
12	boldface and underscored and what-not. So the	11:03:45
13	text of the document is basically encapsulated	11:03:47
14	inside the whole postscript context. There is	11:03:49
15	a lot of declaration stuff at the beginning, if	11:03:55
16	you look through it. And, in particular, if you	11:03:57
17	look at the text version of this document you	11:03:59
18	will find that you will not be able to read this,	11:04:02
19	right? Because the text basically disappears in	11:04:04
20	all the commands.	11:04:09
21	PDF the portable data format is	11:04:10
22	something which was introduced by Adobe later for	11:04:13
23	many reasons. One reason was that postscript	11:04:18
24	turned out not being as portable and as easily	11:04:23
25	reproducible as people like them to I still	11:04:27

1	remember infinite sessions where we spent hours	11:04:31
2	because the printer just wouldn't print that	11:04:35
3	file. It looked fine on screen, you saw	11:04:37
4	everything, it was perfect, but the printer	11:04:41
5	wouldn't print it, or what came out was complete	11:04:42
6	nonsense. Even when I went back to Heidelberg, I	11:04:45
7	still remember a lot of effort we had to put in	11:04:52
8	because, for example, it would happen that	11:04:56
9	a printer disregarded the first command saying,	11:04:58
10	"This is postscript", and then you would end up	11:05:01
11	having 500 pages of postscript commands for	11:05:04
12	a single-page document because sometimes it would	11:05:07
13	even, you know, one-command-per-line kind of	11:05:10
14	nonsense. All of this was a problem because the	11:05:12
15	document which can't reliably print and	11:05:16
16	reproducibly print in every country, big issues	11:05:18
17	between U.S. letter format and European A4, that	11:05:21
18	was solved by introducing PDF, the really	11:05:25
19	portable data format. And postscript is	11:05:28
20	basically not being used anymore. There are	11:05:31
21	converters which are automatically evoked if you	11:05:34
22	open a postscript file and this was why people	11:05:37
23	tend to believe that postscript is basically part	11:05:41
24	of PDF but it's not.	11:05:44
25	Q. Okay, but in '96, if you had	11:05:46

1	a postscript file in the relevant linked	11:05:48
2	references, you could generate something to be	11:05:53
3	printed? Is that what the purpose of postscript	11:05:56
4	files was?	11:05:59
5	MR. DAVIS: Objection; form.	11:06:00
6	THE WITNESS: You would have to	11:06:01
7	download it and then depending on what kind of	11:06:06
8	web browser you had, usually not automatically at	11:06:09
9	this time if I remember correctly, you would have	11:06:12
10	to have a postscript viewer to view this	11:06:14
11	postscript file to have it on screen, and you	11:06:17
12	would have to have a postscript-enabled printer	11:06:19
13	which would understand postscript and those	11:06:22
14	printers were more expensive because they needed	11:06:24
15	a postscript interpreter which is a rather	11:06:26
16	complex piece of software and lots of memory for	11:06:30
17	it to be able then turn this into something on	11:06:32
18	paper.	11:06:35
19	BY MR. BUROKER:	11:06:46
20	Q. Let me show you what's been	11:06:46
21	previously marked as Exhibit 2026 in the '1469	11:06:48
22	IPR proceeding. This is an affidavit of	11:06:59
23	Christopher Butler from the Internet Archive.	11:07:02
24	Have you ever viewed this document as one of the	11:07:05
25	things you considered?	11:07:08

1	A. I have looked at it, yes.	11:07:09
2	Q. Okay, and he attaches materials	11:07:11
3	that were from the Internet Archive from October	11:07:14
4	strike that from January 26th, 1997; is	11:07:26
5	that correct?	11:07:32
6	MR. DAVIS: Objection; form.	11:07:35
7	THE WITNESS: Which particular page are	11:07:38
8	you now referring to?	11:07:40
9	BY MR. BUROKER:	11:07:42
10	Q. I strike that. I'm more	11:07:42
11	interested in the documents that were	11:07:43
12	from October 29, 1996. So it's the one that	11:07:48
13	starts on page 11 of this document.	11:07:53
14	MR. DAVIS: Objection; form.	11:07:59
15	BY MR. BUROKER:	11:08:01
16	Q. 011. So, the question is: in	11:08:03
17	paragraph 6 of his affidavit, he says:	11:08:23
18	"Attached as Exhibit A are true and	11:08:26
19	accurate copies of printouts of the Internet	11:08:28
20	Archive's records of the HTML and PDF files for	11:08:32
21	the URLs and the dates specified in the footer of	11:08:36
22	the printout (for HTML) or on the attached	11:08:40
23	coversheet (for PDF)."	11:08:42
24	MR. DAVIS: Objection; form.	11:08:44
25	///	11:08:46

1	BY MR. BUROKER:	11:08:46
2	Q. Is that what it says?	11:08:46
3	A. This is what is written here, yes.	11:08:49
4	Q. Okay. So on page 11 there's a URL	11:08:53
5	and that's the URL that we were just talking	11:09:01
6	about from your declaration; is that right?	11:09:03
7	MR. DAVIS: Objection; form.	11:09:07
8	THE WITNESS: I would have to compare.	11:09:09
9	If you say so.	11:09:12
10	BY MR. BUROKER:	11:09:15
11	Q. It was paragraph 174.	11:09:15
12	A. Yes.	11:09:17
13	Q. Okay. And then what is attached	11:09:33
14	next, on pages 12 through 49, appears to be the	11:09:36
15	RD24 status report that is the same as the EMC	11:09:46
16	Exhibit 1011 without the library stamp. Do you	11:09:55
17	agree?	11:09:58
18	MR. DAVIS: Objection; form.	11:09:59
19	THE WITNESS: By looking at it I would	11:10:03
20	say so, yes. However, I have not done a direct	11:10:06
21	one-to-one comparison. There may be an earlier	11:10:10
22	version, but since it's dated October 2nd,	11:10:12
23	I would assume so. But please note this is not	11:10:16
24	the entire document, the document was broken up	11:10:18
25	into several pieces, so there is an RD2496_1, _2,	11:10:20

1	_3.	11:10:20
2	BY MR. BUROKER:	11:10:20
3	Q. Right.	11:10:36
4	A. And although I don't know the	11:10:37
5	reason4 even. Let me see, is there another	11:10:39
6	one? I don't remember the reason for doing this.	11:10:43
7	The most likely cause would be this document is	11:10:47
8	filled with pictures and pictures were real full	11:10:52
9	having postscript files to print, or printers to	11:10:55
10	choke when the whole postscript file was	11:10:58
11	submitted, so postscript files then were chopped	11:11:01
12	up into smaller pieces, let alone to be able to	11:11:04
13	print the stuff which would print and isolate the	11:11:06
14	potential error. So this is basically fragments	11:11:11
15	of the whole document.	11:11:14
16	Q. Right.	11:11:16
17	A. But they are all there.	11:11:17
18	Q. Right. In fact there are eight.	11:11:18
19	Page 46 of this has the file header for	11:11:22
20	RD2496_8.ps, correct?	11:11:29
21	A. Eight, yeah, you're right.	11:11:33
22	Q. So if you took the pieces of the	11:11:34
23	document from each of the different RD2496	11:11:36
24	postscript files and put them together, did you	11:11:39
25	do a comparison as to whether that compilation is	11:11:41

1	the same as Exhibit 1011 minus the CERN library	11:11:45
2	stamp?	11:11:50
3	MR. DAVIS: Objection to form.	11:11:51
4	THE WITNESS: I did not do an in-depth	11:11:53
5	comparison whether or not they are word by word	11:11:57
6	the same, but I did check that overall they	11:12:00
7	looked to be the same, same page numbers.	11:12:05
8	Nothing obvious came to mind and I would not see	11:12:08
9	any reason why this would be a different version.	11:12:12
10	BY MR. BUROKER:	11:12:15
11	Q. Right. And so for them to have	11:12:15
12	been for these postscript files to have been	11:12:18
13	gathered by the Internet Archive on October 29th,	11:12:24
14	1996, by that time somebody would have had to	11:12:27
15	place those postscript files on the	11:12:34
16	sunshine.cern.ch:8080 server, correct?	11:12:37
17	MR. DAVIS: Objection; form.	11:12:48
18	THE WITNESS: This archive claims that	11:12:50
19	these documents were downloaded from	11:12:54
20	sunshine.cern.ch:8080. This is what I	11:13:00
21	understand.	11:13:05
22	BY MR. BUROKER:	11:13:06
23	Q. And you have no reason to doubt	11:13:06
24	the Christopher Butler affidavit, do you?	11:13:07
25	A. No, I mean I believe he signed	11:13:10

1	that under oath, right?	11:13:12
2	Q. So do you know who put those	11:13:14
3	postscript files on that sunshine.cern.ch:8080	11:13:19
4	server?	11:13:25
5	A. I don't know but it would be	11:13:28
6	relatively likely that this was Hans Müller, and	11:13:31
7	it was also very possible that because these	11:13:40
8	documents have a certain size particular to	11:13:43
9	postscript that this was the place where	11:13:45
10	everybody was referring to to look at the final	11:13:49
11	document and to say it's all right as part of the	11:13:52
12	work in progress. But remember this is the	11:13:56
13	private web page of the RD24 and not an official	11:13:58
14	generic searchable web page.	11:14:03
15	Q. Well you say it's private but it's	11:14:06
16	on the CERN server, right?	11:14:08
17	A. CERN has about 10,000 computers.	11:14:11
18	So it's one particular computer of one person	11:14:14
19	working at CERN there are 3,000 employees	11:14:19
20	who is using this on a sub-web page which is not	11:14:24
21	part of the official port 80 web pages. So if	11:14:31
22	you would go to www.cern.ch you would not find	11:14:35
23	this, right? This is something else.	11:14:38
24	Q. Well, but CERN owned the computer,	11:14:42
25	right?	11:14:44

1	MR. DAVIS: Objection; form.	11:14:44
2	BY MR. BUROKER:	11:14:44
3	Q. You're trying to draw some	11:14:49
4	distinction and say it's private, but this is	11:14:50
5	a cern.ch address.	11:14:55
6	A. Yeah, but the conclusion you're	11:15:00
7	trying to draw is really wrong. I have computers	11:15:02
8	at CERN worth millions of euros which are owned	11:15:07
9	by the government in Germany because they're paid	11:15:10
10	for by the German Research Council BMBF, but they	11:15:12
11	are at CERN. And since they are for a CERN	11:15:16
12	experiment they are, of course, operating in the	11:15:19
13	CERN computer contacts and if you want to get	11:15:23
14	them they have a CERN network address.	11:15:25
15	Q. But Müller chose to put these on	11:15:29
16	an address that was a cern.ch address and not,	11:15:35
17	you know, drmüller.com or some other URL he could	11:15:38
18	have used, right?	11:15:44
19	MR. DAVIS: Objection; form.	11:15:45
20	THE WITNESS: Every computer at CERN	11:15:51
21	I mean maybe we should enter briefly into a	11:15:54
22	discussion how networks work because I believe	11:15:56
23	there is a misunderstanding here.	11:16:01
24	If I would bring my laptop	11:16:05
25	BY MR. BUROKER:	11:16:07

1	Q. Well that's not an answer to my	11:16:07
2	question, sir. I asked you a question about	11:16:09
3	whether Mr. Müller or Dr. Müller choose to put	11:16:11
4	these on a cern.ch addressed server.	11:16:14
5	MR. DAVIS: Objection; form.	11:16:19
6	THE WITNESS: He put it on a computer	11:16:21
7	which belonged to the RD24 project which was	11:16:23
8	located at CERN and thereby had a CERN network	11:16:30
9	address, like every guest or every person	11:16:33
10	visiting CERN having a CERN network address.	11:16:37
11	Like every person in this room going on to the	11:16:42
12	network, getting a network address in the domain	11:16:44
13	of your law firm.	11:16:48
14	BY MR. BUROKER:	11:16:52
15	Q. Right. And so if I posted	11:16:52
16	something on my firm's network, it wouldn't be my	11:16:55
17	private server, just as this was not really his	11:16:57
18	private server. It's a piece of equipment owned	11:17:00
19	by his employer and on his employer's URL,	11:17:03
20	correct?	11:17:08
21	MR. DAVIS: Objection; form.	11:17:09
22	THE WITNESS: This is what I tried to	11:17:11
23	outline. CERN is not just an employer which owns	11:17:12
24	everything which is part of CERN. CERN is	11:17:17
25	an international organization with lots of highly	11:17:20

1	complicated contracts with lots of entirely	11:17:22
2	autonomously operating organizations. So, for	11:17:27
3	example, the ALICE experiment has nothing to do	11:17:30
4	with CERN although it is located at CERN. We	11:17:33
5	have our own rules, we even have our own bank	11:17:37
6	accounts at CERN, although they are under	11:17:40
7	diplomatic immunity. Nobody can get to these	11:17:44
8	accounts unless the account owner, in one case	11:17:46
9	myself, approves that. Same for the computers.	11:17:48
10	If there is a particular project it has its own	11:17:52
11	set of contacts and ownerships and the fact that	11:17:56
12	the computer are located at CERN only means that	11:18:03
13	they get a CERN address but that doesn't mean	11:18:06
14	that the contents in these computers are owned by	11:18:08
15	CERN or necessarily the computer is owned by	11:18:11
16	CERN. The ownership of sunshine I don't know.	11:18:14
17	RD24 had different funding sources and how the	11:18:17
18	money came together to, for instance, buy those	11:18:23
19	machines, I can't tell at this point, but you	11:18:26
20	cannot automatically draw the conclusion that	11:18:29
21	this is an employee-employee relationship and	11:18:31
22	everything that is under the CERN, inside the	11:18:34
23	CERN domain is owned by CERN.	11:18:37
24	BY MR. BUROKER:	11:18:39
25	Q. But you've drawn a conclusion and	11:18:39

1	given an opinion under oath that it was his	11:18:41
2	private server; is that correct?	11:18:43
3	A. Private server in the sense of the	11:18:45
4	RD24 project, yes. Not private server in the	11:18:47
5	sense he owned it personally privately. This is	11:18:50
6	the RD24 project and in this context his private	11:18:52
7	server, yeah.	11:18:55
8	Q. Often private is used to	11:19:00
9	distinguish between public; was that the	11:19:03
10	distinction you were trying to draw? Or what was	11:19:05
11	the reason why you said it was a private server?	11:19:08
12	MR. DAVIS: Objection to form.	11:19:12
13	THE WITNESS: Both. This is a machine	11:19:18
14	belonging to the RD24 project and the information	11:19:21
15	on there was for the RD24 project, inside the	11:19:26
16	RD24 project, and not for the public and	11:19:31
17	consequently, therefore, I used the word	11:19:36
18	"private".	11:19:39
19	BY MR. BUROKER:	11:19:39
20	Q. Was he an employee of CERN?	11:19:40
21	A. Hans Müller was an employee of	11:19:43
22	CERN, correct.	11:19:45
23	Q. Is he still an employee of CERN?	11:19:46
24	To your knowledge obviously?	11:19:48
25	A. He has reached the age of	11:19:50

1	retirement. He may still be or already have	11:19:52
2	retired but he is still working at CERN, which is	11:19:57
3	rather common. People do research because they	11:20:01
4	like to do that and they keep doing this after	11:20:07
5	their retirement. So he may or may not be at	11:20:09
6	this point.	11:20:12
7	Q. Just to be clear, so we know what	11:20:13
8	the facts are. So what's your understanding as	11:20:16
9	to who owns the cern.ch domain?	11:20:19
10	MR. DAVIS: Objection to form.	11:20:23
11	THE WITNESS: The cern.ch domain is	11:20:28
12	registered by the organization CERN. So from	11:20:33
13	that point of view you can argue that CERN owns	11:20:35
14	it.	11:20:37
15	BY MR. BUROKER:	11:20:50
16	Q. And if I visit a www.cern.ch URL,	11:20:50
17	is that going to be a CERN website?	11:20:59
18	A. That would be the CERN official	11:21:03
19	website, organized by the CERN public relations	11:21:05
20	department, run by the CERN IT department.	11:21:09
21	Q. And the contents of that website	11:21:12
22	would be served off of a CERN server; is that	11:21:13
23	correct?	11:21:13
24	A. That I would assume so to be	11:21:19
25	correct.	11:21:21

1	Q. Are you familiar with the URL	11:21:23
2	cds.cern.ch?	11:21:25
3	A. Where is that?	11:21:32
4	Q. I don't know if it's in your	11:21:35
5	declaration or not.	11:21:37
6	A. Outside the context I may or may	11:21:39
7	not know, I would need to look at it to be sure.	11:21:41
8	Q. It doesn't immediately come to	11:21:47
9	mind as being the CERN Document Server that's	11:21:49
10	associated with the CERN library; is that	11:21:54
11	correct?	11:21:57
12	A. Well, the CERN Document Server	11:21:58
13	I am of course aware, yeah, sure.	11:22:00
14	Q. Okay, so cds.cern.ch is affiliated	11:22:02
15	with the CERN library; is that correct?	11:22:07
16	MR. DAVIS: Objection; form.	11:22:11
17	THE WITNESS: I would assume so. I	11:22:12
18	mean the CERN Document Server means something to	11:22:14
19	me. The short form, how they code that as a URL,	11:22:16
20	I do not know. CERN has a rather complicated	11:22:21
21	document management system which we use. Many,	11:22:24
22	many complex links between different pages which	11:22:30
23	are all residing inside this framework.	11:22:33
24	BY MR. BUROKER:	11:22:40
25	Q. And I think you said before, but	11:22:40

1	let me just clarify it, who owns the computer	11:22:42
2	server that provided the content in the '96	11:22:45
3	timeframe related to the sunshine.cern.ch URL?	11:22:51
4	MR. DAVIS: Objection; form.	11:22:58
5	THE WITNESS: To be correct, I cannot	11:23:02
6	tell. It would be the RD24 project which is	11:23:03
7	a part of CERN but had its own budget, and how	11:23:07
8	the exact financial contributions came about I'm	11:23:11
9	quite sure Dolphin invested something and other	11:23:14
10	companies did, which is very standard at that	11:23:17
11	stage in time, even today; CERN has an entire	11:23:20
12	working group doing this kind stuff. And then	11:23:24
13	Hans Müller may have decided one or the other way	11:23:27
14	how funds are being put together in order to pay	11:23:29
15	this. So that I can't tell after 20 years.	11:23:32
16	BY MR. BUROKER:	11:23:37
17	Q. Do you know who had access in 1996	11:23:37
18	to the sunshine.cern.ch server?	11:23:40
19	MR. DAVIS: Objection; form.	11:23:43
20	THE WITNESS: Hans Müller certainly.	11:23:48
21	I would assume also Hans Bogaerts sorry	11:23:49
22	Andreas Bogaerts B-o-g-a-e-r-t-s who is	11:23:59
23	also an author here. These were two jointly	11:23:59
24	leading the RD24 project. Probably some of the	11:24:07
25	people who worked at CERN with Hans Müller. I	11:24:10

1	don't remember having access except for these	11:24:12
2	private web pages, but I can't really give	11:24:16
3	a complete list.	11:24:20
4	BY MR. BUROKER:	11:24:20
5	Q. Okay. So I just want to clarify	11:24:22
6	that. You do recall visiting the	11:24:24
7	sunshine.cern.ch:8080 pages?	11:24:27
8	A. I probably did.	11:24:32
9	Q. Is it typical in referee	11:24:41
10	publications to cite to something that's	11:24:49
11	confidential in your experience?	11:24:50
12	MR. DAVIS: Objection; form.	11:24:52
13	THE WITNESS: Not really, because	11:24:58
14	a citation is there to give a second reference to	11:25:01
15	back up an argument and if it's confidential and	11:25:04
16	you cannot use this it would be difficult.	11:25:07
17	But it can happen that such citations	11:25:16
18	are being made and certain particular access is	11:25:20
19	given. So, for example, we have these cases	11:25:24
20	happening from time to time if there is a PhD	11:25:27
21	thesis written as a joint project with industry,	11:25:30
22	and the thesis contains material which is, for	11:25:35
23	example, subject to a patent just being in the	11:25:38
24	process of being filed and the thesis is declared	11:25:42
25	confidential, although a thesis has to be	11:25:45

1	published one can put a certain timeframe on it	11:25:47
2	saying it will remain unpublished for a certain	11:25:50
3	time until, for example, all the IP has been	11:25:53
4	filed and the submission of the thesis is not	11:25:56
5	damaging any more to the IP. So this "no" has to	11:25:58
6	be taken with a grain of salt.	11:26:07
7	(Exhibit No. EMC 1027 was marked for	11:26:07
8	identification.)	11:26:20
9	BY MR. BUROKER:	11:26:20
10	Q. And I believe we're on the same	11:26:20
11	numbering scheme for both IPRs on the 1000	11:26:21
12	series, so this is 1027 in both proceedings.	11:26:25
13	Actually, yeah, we'll just make it 1027 in both	11:26:31
14	proceedings just to make it easier.	11:26:38
15	MR. DAVIS: Okay. I'm going to make	11:26:39
16	some evidentiary objections. It's outside the	11:26:40
17	scope of direct of institution. I can't tell if	11:26:43
18	it's incomplete or not. I think it's irrelevant,	11:26:48
19	may be prejudicial, likely hearsay, lacks	11:26:54
20	authentication and may contain improper opinion	11:26:58
21	evidence.	11:27:03
22	BY MR. BUROKER:	11:27:07
23	Q. Okay, Dr. Lindenstruth, have you	11:27:07
24	ever seen this before?	11:27:11
25	A. I do not remember.	11:27:13

1	Q. Is the Hans Müller the same Hans	11:27:16
2	Müller we've been talking about? Was he	11:27:19
3	affiliated with the CERN EP Electronic Design	11:27:21
4	Group?	11:27:24
5	A. Well I mean it states so on this	11:27:28
6	document so I have no reason to doubt that,	11:27:32
7	although CERN is constantly restructuring. The	11:27:36
8	EP Group was or is a really large group. It is	11:27:41
9	well possible that he was a member of that group	11:27:44
10	at that time.	11:27:46
11	Q. Do you know what an LHC-B note is?	11:27:48
12	A. You're referring to the header of	11:27:59
13	the document LHC-B?	11:28:02
14	Q. Yes, the header says:	11:28:04
15	"LHC-B Note 98-030."	11:28:07
16	So I was asking if you knew what	11:28:11
17	an LHC-B note is.	11:28:17
18	A. CERN has four major experiments	11:28:18
19	for its LHC accelerator, right? One has to	11:28:24
20	disentangle the accelerator, we call that the	11:28:28
21	machine, and then the experiments. The physics	11:28:31
22	is done at the experiments. There are four	11:28:33
23	experiments: ALICE; ATLAS; CMS; and LHC-B.	11:28:35
24	LHC-B, an obviously very creative name, was	11:28:47
25	chosen because LHC studies the weak interaction,	11:28:52

1	which is very important for understanding some of	11:28:59
2	the fundamental principles of our being here.	11:29:03
3	The B meson m-e-s-o-n is a particle which	11:29:09
4	decays weakly interacting and is extremely rare	11:29:18
5	and one needs these extremely powerful	11:29:24
6	accelerators to create them and then LHC-B was	11:29:27
7	built to basically study the decay of this B	11:29:31
8	meson. So since it's the LHC-B experiment, then	11:29:35
9	you see there are variants of noting, the title	11:29:39
10	says "LHCb" without dash, the note says "LHC-B"	11:29:44
11	with a dash. I assume this is a note of the	11:29:47
12	LHC-B experiment with a reference number. If it	11:29:51
13	was a document for the ALICE experiment, it would	11:29:58
14	be "ALICE Note" with such a number and so forth.	11:30:00
15	Q. Well who are these notes what	11:30:03
16	are these notes created for?	11:30:05
17	MR. DAVIS: Objection; form, outside	11:30:08
18	the scope.	11:30:11
19	THE WITNESS: Now, yeah, I'm not	11:30:13
20	a member of the LHC-B collaboration and I'm	11:30:15
21	seeing this for the first time. I can only draw	11:30:18
22	a conclusion from my experience how it works in	11:30:22
23	ALICE experiment, which is not uncommon.	11:30:25
24	Standard procedure is if you wish to make	11:30:30
25	a statement to the collaboration we're	11:30:33

1	talking, again, this group preparing the	11:30:36
2	experiment saying, "This is the particular way	11:30:40
3	something could work, this is a suggestion to	11:30:44
4	solve a particular problem", then normally one	11:30:51
5	writes up a note, which is basically an internal	11:30:54
6	paper, which is submitted to that particular	11:30:59
7	collaboration for review.	11:31:05
8	Notes are, as far as I know, never	11:31:11
9	publications, they are used for internal they	11:31:14
10	are made for internal use as a reference to	11:31:15
11	discuss something particular.	11:31:18
12	BY MR. BUROKER:	11:31:27
13	Q. So, if you look at the references	11:31:28
14	in this document. Reference 6 cites to the RD24	11:31:29
15	status report 1996, LHCC 96-33 October 1996, and	11:31:40
16	then it's got the URL http://sunshine.cern.ch:	11:31:48
17	8080/RD24/rd24.html. Do you see that?	11:31:59
18	A. Yeah.	11:32:07
19	Q. So in 1998, in a note to the	11:32:08
20	LHC-B, Hans Müller is citing to that	11:32:14
21	sunshine.cern.ch:8080 server reference which	11:32:17
22	appears to have the RD24 status report from 1996,	11:32:23
23	correct?	11:32:27
24	MR. DAVIS: Objection; form.	11:32:28
25	THE WITNESS: Well it is printed here.	11:32:31

1	More I cannot say about that.	11:32:33
2	BY MR. BUROKER:	11:32:37
3	Q. That doesn't suggest to you	11:32:37
4	well, first of all, you have never this document	11:32:38
5	before?	11:32:41
6	A. No, I don't think so.	11:32:42
7	Q. Okay. So you didn't consider this	11:32:44
8	in your declaration when you gave the opinion you	11:32:46
9	thought that the RD24 document was kept	11:32:50
10	confidential, correct?	11:32:53
11	In other words, you didn't have this	11:32:56
12	when you made that determination?	11:32:57
13	A. Your second statement is correct,	11:33:00
14	yes, I didn't have this when I made my	11:33:01
15	declaration.	11:33:05
16	Q. Okay. And reference number 18 in	11:33:05
17	this list of references also says:	11:33:09
18	"Applications of SCI to Data	11:33:12
19	Acquisition at LHC"	11:33:21
20	which is the same title as	11:33:22
21	Exhibit 1011, the RD24 status report, right?	11:33:25
22	MR. DAVIS: Objection to form.	11:33:28
23	THE WITNESS: Yeah, but I mean this is	11:33:36
24	only referencing the RD24 home page, which is	11:33:37
25	still using this private port number on the	11:33:41

1	website of Hans Müller, yeah. On this sunshine	11:33:47
2	machine, yeah.	11:33:51
3	BY MR. BUROKER:	11:33:53
4	Q. All right, but he's citing to this	11:33:53
5	port on this URL to a working group that's not	11:33:56
6	the RD24 working group, he's citing it to the	11:34:02
7	LHC-B group, correct?	11:34:05
8	A. Yet another CERN internal working	11:34:10
9	group, yeah.	11:34:12
10	Q. So at a minimum he doesn't think	11:34:13
11	that the document is confidential only to the	11:34:14
12	RD24 working group?	11:34:17
13	MR. DAVIS: Objection to form.	11:34:19
14	BY MR. BUROKER:	11:34:21
15	Q. Correct?	11:34:21
16	MR. DAVIS: Calls for improper opinion	11:34:22
17	evidence.	11:34:24
18	THE WITNESS: I mean, since you're	11:34:32
19	referring several times to confidentiality, I	11:34:34
20	should probably outline why I said that this is	11:34:36
21	subject to confidentiality.	11:34:41
22	BY MR. BUROKER:	11:34:43
23	Q. Your counsel can ask you that	11:34:43
24	question, I want an answer to my question which	11:34:44
25	is that this document suggests that at least	11:34:46

1	Mr. Müller didn't believe that the RD24 status	11:34:55
2	report had to be kept confidential within the	11:34:59
3	RD24 working group because he cited it to	11:35:00
4	an outside CERN group.	11:35:04
5	A. This is a CERN group.	11:35:08
6	Q. To another CERN group?	11:35:09
7	MR. DAVIS: Objection; form. And I	11:35:09
8	maintain my evidentiary objection.	11:35:11
9	THE WITNESS: Again, it all depends on	11:35:18
10	the particular confidentiality agreement which	11:35:20
11	was signed.	11:35:21
12	BY MR. BUROKER:	11:35:23
13	Q. I'm just talking about, doesn't	11:35:23
14	this suggest that at least Dr. Müller I said	11:35:25
15	Mr. Müller it's Dr. Müller he has cited the	11:35:29
16	RD24 status report to a different working group	11:35:32
17	within CERN, correct?	11:35:36
18	MR. DAVIS: Objection; form.	11:35:41
19	THE WITNESS: That document was given	11:35:44
20	to apparently somebody else, a different group	11:35:49
21	inside CERN working under possibly the same	11:35:52
22	confidentiality requirements.	11:35:58
23	BY MR. BUROKER:	11:36:03
24	Q. Do you know how many people were	11:36:03
25	involved in the LHC-B working group in 1996 to	11:36:04

1	1998?	11:36:09
2	A. I do not. I see this document for	11:36:10
3	the first time, I can't tell you.	11:36:12
4	Q. But this is a different question.	11:36:14
5	Do you know, based on your work at CERN, do you	11:36:15
6	know how many people were involved in the LHC-B	11:36:18
7	working group in the '96 to '98 timeframe?	11:36:21
8	A. I mean it would have to be the	11:36:26
9	group focusing at data acquisition and online	11:36:28
10	data selection. I don't know the size of that	11:36:35
11	group. From my experience it would be a rather	11:36:39
12	small group, handful of people. But this is	11:36:43
13	a guess and I don't wish to raise guesses here,	11:36:47
14	so I can't give you a clear answer as how many	11:36:50
15	people have been involved here, but we're not	11:36:54
16	talking huge collaborations.	11:36:56
17	Q. Do you know if Dr. Müller was	11:37:00
18	involved in both RD24 and the LHC-B working	11:37:01
19	groups?	11:37:09
20	A. I mean, in general, these RD	11:37:09
21	projects were not there to work for any	11:37:12
22	particular experiment, they were there to solve	11:37:16
23	generic problems for basically the entire LHC	11:37:18
24	project. This is why they're called RD and not	11:37:22
25	experiment A, B, C, D, right? And so it was well	11:37:25

1	within hi	s obl	igations to, let's say, market the	11:37:29
2	technolog	y to	possibly interested other groups	11:37:34
3	helping t	hem t	o solve their particular computing	11:37:39
4	problems.	So	apparently he's trying to address	11:37:42
5	an issue	which	is particular for the LHC-B	11:37:50
6	experimen	t, sh	owing a potential solution. But	11:37:56
7	without r	eferr	ing to this document in depth	11:38:00
8	and I wou	ld ha	ve to read it carefully, we're	11:38:03
9	talking s	ome 1	9 pages I can't tell more.	11:38:05
10	(Brief pau	ise to	re-establish realtime connections.)	11:39:39
11	BY MR. BU	ROKER	:	11:39:39
12		Q.	Dr. Lindenstruth, I want to turn	11:39:40
13	you to pa	ge 8	and paragraph 20 of your '814	11:39:40
14	declarati	on.		11:39:45
15		So th	ne first sentence says you	11:39:57
16	understan	d tha	t in Inter Partes Review, the claim	11:40:00
17	terms are	to b	e given their broadest reasonable	11:40:03
18	interpret	ation	in light of the specification,	11:40:06
19	correct?			11:40:08
20		Α.	Yeah.	11:40:09
21		Q.	And that's your understanding	11:40:09
22		Α.	Yeah.	11:40:12
23		Q.	provided by counsel, correct?	11:40:12
24		Α.	(The witness nodded.)	11:40:14
25		Q.	You have to say "yes" or "no", so	11:40:16

1	she can have an answer.	11:40:19
2	A. Yes.	11:40:20
3	Q. Or some audible response. Okay.	11:40:21
4	I think there we might have identified	11:40:27
5	one of those typos and I just want to clarify	11:40:30
6	that.	11:40:32
7	So the next sentence say:	11:40:32
8	"In performing my analysis and	11:40:34
9	rendering my opinions, where the Board of	11:40:36
10	Acqis"	11:40:38
11	I think that should be "or Acqis"	11:40:39
12	but you tell me	11:40:43
13	" has proposed a construction of the	11:40:44
14	BRI of a claim term, I have applied that	11:40:59
15	construction in my analysis."	11:40:49
16	Should that be "Board or Acqis"?	11:40:50
17	A. Well, for all the broadest	11:41:01
18	reasonable interpretation cases and further I	11:41:02
19	have referred to the Board. So in my	11:41:04
20	understanding this is the Board for this Acqis	11:41:06
21	case, and not written	11:41:07
22	Q. Oh, is that what you meant? Okay.	11:41:10
23	It wasn't clear whether you meant the Board	11:41:13
24	meaning like Board of Directors of Acqis or you	11:41:15
25	meant Board of Patent Appeals or Acqis. So	11:41:17

1	what's your	11:41:21
2	A. No, I've referred, I mean, to what	11:41:22
3	the Board has said in some of the cases which are	11:41:27
4	discussed further, right? It's either the	11:41:29
5	decision of the Board or what I would consider,	11:41:34
6	as an expert in this field, to be the broadest	11:41:36
7	reasonable interpretation.	11:41:41
8	Q. But I believe there are some	11:41:42
9	instances in which Acqis has proposed a broadest	11:41:45
10	reasonable interpretation.	11:41:52
11	A. Inside the patent, yes.	11:41:52
12	Q. Correct. And you used Acqis's	11:41:54
13	proposed broadest reasonable interpretation in	11:41:58
14	a few instances as well, correct?	11:42:00
15	A. If as set forth inside the patent	11:42:02
16	documents, correct.	11:42:05
17	Q. What patent documents are you	11:42:06
18	talking about? Just so we're on the same page.	11:42:09
19	Do you mean in the patents themselves?	11:42:11
20	A. Yeah, as we refer here to the '814	11:42:12
21	then it would have to be the '814 document,	11:42:15
22	you're right.	11:42:19
23	Q. Okay, I just want to make sure I	11:42:19
24	understand so we're clear for the record, because	11:42:21
25	there's different patent documents: there's the	11:42:24

1	patent, there's the file history. Just so we're	11:42:28
2	clear I may ask you to clarify what we're talking	11:42:30
3	about, okay?	11:42:32
4	And then it says:	11:42:33
5	"Otherwise, I have interpreted claim	11:42:41
6	terms by giving them the ordinary meaning that	11:42:42
7	they would have to a [person of skill in the	11:42:46
8	art], reading the '814 patent with its priority	11:42:48
9	filing date (October 30, 1998) in mind, and in	11:42:53
10	light of its specification and file history."	11:42:57
11	Do you see that?	11:43:03
12	A. I see that, yes.	11:43:03
13	Q. So just to be clear, if the Board	11:43:04
14	gave an interpretation of what it found to be the	11:43:07
15	broadest reasonable interpretation, you applied	11:43:10
16	the Board's interpretation correct?	11:43:12
17	A. Correct.	11:43:14
18	Q. If you don't have a Board	11:43:15
19	interpretation then you used the ordinary meaning	11:43:16
20	of the term or the broadest reasonable	11:43:20
21	interpretation of the remaining terms?	11:43:24
22	MR. DAVIS: Objection to form.	11:43:28
23	BY MR. BUROKER:	11:43:30
24	Q. Or do you think they mean the same	11:43:31
25	thing? The ordinary meaning means the same thing	11:43:32

1	as broadest reasonable interpretation?	11:43:34
2	MR. DAVIS: Objection to form.	11:43:36
3	THE WITNESS: The broadest reasonable	11:43:40
4	interpretation in light of the specification.	11:43:45
5	This is what I used.	11:43:46
6	BY MR. BUROKER:	11:43:48
7	Q. So where it says "ordinary	11:43:48
8	meaning" what you meant is the broadest	11:43:49
9	reasonable interpretation in light of the	11:43:53
10	specification of the term?	11:43:53
11	A. It's my understanding this is what	11:43:56
12	I'm supposed to do.	11:43:57
13	Q. All right, it wasn't clear and	11:43:59
14	that's why I wanted to ask that question.	11:44:00
15	THE WITNESS: I would like to go to the	11:44:04
16	bathroom one more time.	11:44:06
17	MR. BUROKER: The bathroom again?	11:44:08
18	Sure.	11:44:09
19	THE WITNESS: Yes, it's almost 12:00	11:44:10
20	now.	11:44:12
21	MR. BUROKER: Yes, let's go off the	11:44:13
22	record.	11:44:14
23	(Brief recess taken 11:44 a.m 11:51 a.m.)	11:51:49
24	BY MR. BUROKER:	11:51:49
25	Q. So, turning then to paragraph 114.	11:51:53

1	MR. DAVIS: Just to be clear we're	11:52:04
2	still on the '814.	11:52:05
3	MR. BUROKER: Yeah, I'm using that as	11:52:08
4	the primary document. I know that they're very	11:52:09
5	similar.	11:52:12
6	BY MR. BUROKER:	11:52:17
7	Q. So actually I was going to	11:52:12
8	paragraph 113, sorry.	11:52:15
9	So in Section VII, "Claim Construction",	11:52:17
10	you set forth your discussion of three terms that	11:52:21
11	you specifically identified as providing	11:52:29
12	construction for; is that correct?	11:52:37
13	A. Yeah, this is correct.	11:52:37
14	Q. And that's the "peripheral	11:52:39
15	component interconnect (PCI) bus transaction"	11:52:41
16	term, the "encoded" term and then the "extending	11:52:42
17	from" term, correct?	11:52:45
18	A. This is correct.	11:52:46
19	Q. Okay. For the "PCI bus	11:52:47
20	transaction" term, if I use that phrase you'll	11:52:54
21	know which one I'm referring to rather than	11:52:56
22	repeating the whole thing, right? So I'll just	11:53:01
23	say "PCI bus transaction".	11:53:03
24	A. (The witness nodded.)	11:53:04
25	Q. Okay. So for the "PCI bus	11:53:06

1	transaction" term, you say that:	11:53:09
2	" [the] Board construed the terms to	11:53:12
3	mean 'Peripheral Component Interconnect	11:53:15
4	industry standard bus transaction."	11:53:20
5	Correct?	11:53:21
6	A. Yeah.	11:53:22
7	Q. So that's the interpretation you	11:53:22
8	used as the broadest reasonable interpretation?	11:53:24
9	A. Uh-huh, yes.	11:53:27
10	Q. But then you provide some	11:53:28
11	additional thoughts on what that means in	11:53:31
12	paragraph 114, right?	11:53:34
13	A. Yeah, it seemed important.	11:53:49
14	Q. Okay. So you say that a PCI bus	11:53:51
15	transaction must include the PCI address and bus	11:54:11
16	command information during the address phase and	11:54:20
17	the PCI data byte enables during the data phase.	11:54:23
18	Is that your understanding?	11:54:27
19	A. Amongst other things, yes.	11:54:30
20	Although I just don't see it where I wrote this	11:54:32
21	in detail.	11:54:37
22	Q. Well let me look for it, too. Oh	11:54:38
23	here it is. So the second line on page 77 after	11:54:54
24	the semicolon, you say:	11:54:56
25	" they require the address and data	11:55:01

1	phases of a PCI bus transaction, which includes	11:55:03
2	the PCI address and bus command information	11:55:06
3	during the address phase"	11:55:09
4	And then you cite to the PCI spec and	11:55:11
5	then you say:	11:55:14
6	" and the PCI data and byte enables	11:55:15
7	during the data phases."	11:55:17
8	Do you see that?	11:55:19
9	A. That is correct, yeah, yeah.	11:55:20
10	Q. When you say "they", you are	11:55:22
11	referring to the claims? You can read the whole	11:55:26
12	sentence but I'm trying to understand what you	11:55:30
13	mean when you say "they require".	11:55:32
14	A. In the claims discuss	11:55:40
15	communicating PCI transactions, so the claims do	11:55:42
16	not require the PCI bus transactions occur on	11:55:50
17	a PCI bus, they require the address and data	11:55:53
18	phases and so forth. So the "they" in this	11:55:56
19	context refers to the claims to make clear that	11:56:01
20	what PCI bus transaction really has to include.	11:56:06
21	Q. So is it your understanding that	11:56:14
22	you need to communicate the PCI address and bus	11:56:20
23	command information during an address phase and a	11:56:25
24	PCI data and byte enables during the data phase	11:56:28
25	to have communicated a PCI bus transaction?	11:56:33

1	A. Yes. If you would leave any of	11:56:37
2	those out it cannot work. For example, if you	11:56:41
3	leave the command out, the target being addressed	11:56:45
4	wouldn't know where the read is or the write is	11:56:49
5	or the configuration and so forth, that has to be	11:56:51
6	there. And there is even more context which is	11:56:55
7	set forth in the PCI specification, which has to	11:56:59
8	be there for a PCI transaction to function.	11:57:03
9	Q. Okay. I'm just trying to	11:57:07
10	understand. That's the understanding of the term	11:57:08
11	"PCI bus transaction" that you used in analyzing	11:57:15
12	the claims as compared to the prior art that was	11:57:20
13	asserted in these IPRs, correct?	11:57:23
14	A. Yeah.	11:57:27
15	Q. So let's look at the claims. So	11:57:27
16	that's the '814 patent which is the 1001 from the	11:57:45
17	'1469 IPR. And then I'll give you the '873	11:57:55
18	Patent which is 1001 from the '1462 IPR.	11:58:01
19	THE WITNESS: Oops they have the same	11:58:09
20	reference number.	11:58:11
21	BY MR. BUROKER:	11:58:11
22	Q. Right, they do, because of the	11:58:12
23	weird way in which the PTO PTAB procedures	11:58:13
24	require that we number exhibits. So rather than	11:58:15
25	use the exhibit number, if we just talk about	11:58:19

1	which patent you're looking at.	11:58:21
2	So looking at the '814 Patent, claim 24,	11:58:24
3	let's start down with the element that says,	11:58:45
4	"a second LVDS channel". Do you see that one?	11:58:52
5	It's the sixth or seventh one down.	11:58:55
6	A. Yeah.	11:58:55
7	Q. Okay, so one of the elements of	11:58:59
8	the claim talks about:	11:58:59
9	"A second LVDS channel comprising two	11:59:00
10	unidirectional serial channels that transmit data	11:59:05
11	in opposite directions, said second LVDS channel	11:59:07
12	extending from said north bridge"	11:59:13
13	and it says:	11:59:16
14	" to convey said address and data	11:59:16
15	bits of PCI bus transaction in serial form."	11:59:20
16	Do you see that?	11:59:25
17	A. I see that.	11:59:29
18	Q. And then up in the northbridge	11:59:29
19	limitation, a couple of limitations up, it says:	11:59:31
20	"A north bridge to communicate address	11:59:33
21	and data bits of PCI bus transaction in serial	11:59:36
22	form"	11:59:40
23	Do you see that?	11:59:40
24	A. Ah, here we are, yes.	11:59:46
25	Q. Okay. So in both of those	11:59:49

1	limitations there's this phrase "address and data	11:59:51
2	bits of PCI bus transaction in serial form".	11:59:55
3	A. Uh-huh.	12:00:01
4	Q. Right?	12:00:02
5	A. Yes.	12:00:02
6	Q. So you agree that that phrase uses	12:00:03
7	the singular form of the word "transaction",	12:00:10
8	correct?	12:00:14
9	A. Yes.	12:00:24
10	Q. So it doesn't say "transactions",	12:00:25
11	it just says "transaction", correct?	12:00:27
12	A. It says that, yeah.	12:00:31
13	Q. Okay. So that would cover	12:00:32
14	a situation in which a single transaction is	12:00:36
15	communicated, right?	12:00:42
16	A. Well, I mean, in any particular	12:00:45
17	case only one PCI transaction can occur at any	12:00:47
18	point in time. It's a bus.	12:00:51
19	Q. But the claim doesn't require that	12:00:54
20	the northbridge communicate multiple bus	12:00:56
21	transactions, it just has to, at any point in	12:01:01
22	time, communicate one to meet this claim, right?	12:01:04
23	MR. DAVIS: Objection to form.	12:01:08
24	THE WITNESS: The PCI specification	12:01:10
25	lays out how a PCI transaction has to work, and	12:01:14

1	according to the specification at any point in	12:01:19
2	time there is one PCI transaction ongoing on the	12:01:21
3	bus.	12:01:23
4	BY MR. BUROKER:	12:01:24
5	Q. Right, and I'm asking you	12:01:25
6	a question more about how you read these claims.	12:01:26
7	So claim 24 is a method claim. It's your	12:01:28
8	understanding that a method claim understands	12:01:34
9	multiple steps that are performed, right?	12:01:36
10	A. Uh-huh.	12:01:38
11	Q. Okay. And one of those steps is	12:01:38
12	inserting an attached computer module into the	12:01:48
13	bay of a console and then the rest of this claim	12:01:52
14	not the rest but a lot of the other elements	12:01:56
15	then specify what is inside the ACM, the attached	12:01:58
16	computer module, right?	12:02:04
17	A. Uh-huh.	12:02:05
18	Q. And that's, you know, the	12:02:06
19	microprocessor, northbridge, main memory and	12:02:08
20	second LVDS channel are part of the ACM. Is that	12:02:11
21	the right way you read this claim?	12:02:16
22	MR. DAVIS: Objection to form.	12:02:18
23	THE WITNESS: "Modular computing	
24	system, the console comprising a first LVDS	
25	signal differential signal channel comprising	

1	two unidirectional serial channels that transmit	
2	encoded data of PCI Component Interconnect	
3	bus transaction in opposite directions."	
4	Yes, this is what it says. It goes on:	12:02:41
5	"A microprocessor unit coupled to a	12:02:41
6	mass memory storage device;	12:02:41
7	A north bridge to communicate address	12:02:47
8	and data bits."	12:02:48
9	This is the claim.	12:02:49
10	BY MR. BUROKER:	12:02:49
11	Q. Right. But the way this claim is	12:02:52
12	structured, just so we are on the same page, is	12:02:54
13	that the microprocessor, northbridge, main memory	12:02:56
14	and second LVDS channel are defined what has to	12:03:00
15	be part of the ACM, correct?	12:03:07
16	MR. DAVIS: Objection to form.	12:03:10
17	THE WITNESS: The ACM comprises	12:03:13
18	a microprocessor coupled to a mass storage	12:03:16
19	device, the northbridge, communicating the data	12:03:18
20	bits in serial form, comprises a main memory,	12:03:22
21	coupled to the microprocessor unit through the	12:03:27
22	northbridge and the second LVDS channel. Yeah.	12:03:30
23	BY MR. BUROKER:	12:03:30
24	Q. Right, okay. So the northbridge	12:03:34
25	part of the ACM has to communicate address and	12:03:41

1	data bits of PCI bus transaction in serial form,	12:03:47
2	right?	12:03:51
3	A. Yeah.	12:03:54
4	Q. It doesn't say that it has to	12:03:54
5	communicate multiple PCI bus transactions in	12:03:56
6	serial form, it can but it doesn't have to do	12:03:59
7	multiple ones. Is that your understanding of how	12:04:03
8	to read this claim?	12:04:05
9	A. I don't understand the	12:04:08
10	differentiation you're trying to make here. If	12:04:09
11	the northbridge is capable of performing a PCI	12:04:16
12	transaction, a PCI is a defined standard. In	12:04:19
13	order to be compliant with that standard it has	12:04:24
14	to be capable of performing all the functionality	12:04:28
15	set forth by the standard or it would be	12:04:30
16	incompatible and it would not be allowed to use	12:04:32
17	the term. So that means, of course, one cannot	12:04:35
18	limit this claim to saying if there is one single	12:04:38
19	particular PCI transaction executed or capable of	12:04:41
20	if the northbridge is capable of doing just	12:04:46
21	one particular transaction and not the features	12:04:48
22	as defined by PCI, that would not be a correct	12:04:54
23	interpretation. So this is why I'm a little	12:04:59
24	confused why you're trying to disentangle between	12:05:01
25	singular and plural here.	12:05:04

1	Q. So that's the way you read this	12:05:07
2	northbridge limitation, the way you've just	12:05:08
3	explained it then?	12:05:11
4	A. (The witness nodded.)	12:05:13
5	Q. Okay. Now, the claim says that	12:05:14
6	you have to communicate address and data bits.	12:05:17
7	You would agree with me that it doesn't mention	12:05:22
8	command information, correct?	12:05:25
9	MR. DAVIS: Objection to form.	12:05:28
10	THE WITNESS: It says:	12:05:31
11	" address and data bits of PCI	12:05:34
12	transaction in serial form"	12:05:37
13	It doesn't say explicitly the other	12:05:38
14	corollary information which is needed to define	12:05:41
15	a PCI transaction, but it says "PCI transaction".	12:05:44
16	So without, for instance, the additional	12:05:48
17	functionality, it wouldn't be a PCI transaction.	12:05:55
18	BY MR. BUROKER:	12:06:10
19	Q. So even though the word "command	12:06:10
20	information" is not expressly present, it's your	12:06:12
21	reading of this claim that the northbridge must	12:06:15
22	communicate PCI bus command information in serial	12:06:20
23	form as well; is that correct?	12:06:24
24	A. If you read this patent you will	12:06:28
25	find that this context is defined as such. It is	12:06:30

1	about a PCI transaction.	12:06:34
2	Q. Okay. The claim also doesn't	12:06:35
3	expressly require transmission or communication	12:06:40
4	of what you call byte enables either, does it?	12:06:43
5	A. It doesn't explicitly state, yes.	12:06:49
6	Q. But, again, it's your	12:06:52
7	understanding that to meet this claim the	12:06:53
8	northbridge must communicate byte enables from	12:06:57
9	a PCI bus transaction, correct?	12:07:03
10	MR. DAVIS: Objection; form.	12:07:05
11	THE WITNESS: There is signals on the	12:07:08
12	PCI bus, data bus signals, which are invalid	12:07:10
13	because of byte enables being set to invalid. So	12:07:14
14	this has to be encoded in some form, otherwise	12:07:20
15	the data, again, has no meaning.	12:07:23
16	BY MR. BUROKER:	12:07:27
17	Q. And the phrasing here also doesn't	12:07:28
18	say that you have to communicate all of the	12:07:32
19	address and data bits of a PCI bus transaction.	12:07:36
20	Do you agree?	12:07:41
21	A. It doesn't explicitly say that,	12:07:43
22	but, again, if I give you a telephone number but	12:07:47
23	leave out two digits, what relevance does it	12:07:53
24	have?	12:07:58
25	Q. Right. So, in your view, if the	12:08:00

1	northbridge did not communicate all of the	12:08:04
2	address and data bits and all of the command	12:08:07
3	information and byte enables of a PCI bus	12:08:09
4	transaction in serial form, you would believe	12:08:14
5	that that northbridge doesn't meet this claim	12:08:17
6	limitation; is that correct?	12:08:20
7	A. It wouldn't be a PCI bus	12:08:21
8	transaction.	12:08:23
9	Q. Well, the question is: if the	12:08:23
10	northbridge didn't communicate all of the address	12:08:26
11	and data bits and all of the bus command	12:08:30
12	information and byte enables but only	12:08:33
13	communicated some of those bits, in your view it	12:08:36
14	wouldn't meet this claim's requirement, right?	12:08:39
15	A. I believe that's correct, yeah.	12:08:43
16	Q. And you say you're getting that	12:08:45
17	from reading the specification. Do you cite	12:08:51
18	anywhere in this explanation where the	12:08:59
19	specification dictates that or is it from the PCI	12:09:01
20	specification alone? Let me strike that because	12:09:06
21	the word "specification" is confusing.	12:09:10
22	Are you getting that from the	12:09:12
23	requirements of the PCI specification or the	12:09:14
24	patent specification or both?	12:09:17
25	MR. DAVIS: Objection; form.	12:09:22

1	THE WITNESS: First, this is in the	12:09:25
2	context of a PCI bus transaction and this is well	12:09:27
3	defined, if you leave something out, remove	12:09:31
4	something, then it is not, again, according to	12:09:33
5	the specification, it wouldn't function and also	12:09:37
6	looking at the problem the patent solves would	12:09:43
7	require this information to be there.	12:09:48
8	BY MR. BUROKER:	12:09:50
9	Q. Okay, let me give you then, just	12:09:51
10	in case you need it, the	12:09:52
11	A. The PCI local bus specification	12:09:58
12	2.1.	12:09:58
13	BY MR. BUROKER:	12:10:00
14	Q. This is Exhibit 2001, I'm not sure	12:10:00
15	if it's in both or which of the it's 2001 in	12:10:03
16	one of the two IPR proceedings.	12:10:08
17	MR. DAVIS: I think it's in both, but	12:10:10
18	I'm not positive on that.	12:10:12
19	BY MR. BUROKER:	12:10:14
20	Q. Okay, I think so too.	12:10:15
21	But anyway you've seen this before	12:10:16
22	obviously.	12:10:21
23	A. Yeah.	12:10:22
24	Q. Okay. And this is PCI Spec Rev	12:10:22
25	2.1 that's referred to in your declaration	12:10:26

1	paragraph 114; is that right?	12:10:29
2	A. 114 I have to verify but, yes,	12:10:33
3	it's certainly being referenced.	12:10:36
4	Q. Sorry, you have multiple documents	12:10:36
5	open at once. Do you have that?	12:10:36
6	A. Yeah. And I believe there is some	12:10:45
7	language about what is the correct version of the	12:10:49
8	PCI local bus specification because this thing	12:10:52
9	has been a little bit iterative. The 2.2 I	12:10:58
10	believe was followed around '99/2000, I don't	12:11:03
11	remember exactly. Although the changes, the	12:11:06
12	differences between 2.1 and 2.2 are minor and not	12:11:09
13	relevant here, but just to be correct. I think	12:11:12
14	it's on page 30.	12:11:15
15	Q. And so you're oh, go ahead,	12:11:22
16	you're still answering.	12:11:25
17	A. 2.1 is the relevant one being	12:11:42
18	valid at the time.	12:11:46
19	Q. Right. So in paragraph 114 you	12:11:47
20	cite to page 30 of this PCI specification	12:11:49
21	Exhibit 2001. So can you point me to which	12:12:00
22	particular portion of page 32 you were	12:12:06
23	A. 30 or 32?	12:12:09
24	Q. It says 32 in your declaration.	12:12:10
25	A. I'm just trying to find the	12:12:43

1	context so it is clear.	12:12:44
2	Q. And if it's meant to be	12:12:46
3	a different page we can correct it, that's one of	12:12:47
4	the reasons I asked that question. I'm not sure	12:12:49
5	that that's anyway, I'll let you testify.	12:12:50
6	My question is which portion of the PCI	12:12:52
7	Spec Revision 2.1 supports your view that the	12:12:54
8	claims require the address and data phases of the	12:13:01
9	PCI bus transaction which include the PCI address	12:13:05
10	and bus command information during the address	12:13:07
11	phase and the PCI data and byte enables during	12:13:10
12	the data phases?	12:13:13
13	A. I mean these references are meant	12:13:15
14	to be examples in any case because when we're	12:13:16
15	talking about a PCI, then this is what it is,	12:13:21
16	right? Like, with every interface document or	12:13:23
17	standard this is a de facto standard if you	12:13:29
18	violate parts of it you don't have a standard	12:13:34
19	anymore and it doesn't work anymore because the	12:13:37
20	reason for this is to enable different devices to	12:13:39
21	communicate.	12:13:42
22	Now, this reference here is about the	12:13:43
23	requirement that there is address and command	12:13:44
24	information during the address phase at 32. So	12:13:47
25	let me just see, this is a long page of text it	12:13:51

1	must be in here. Let me look this up.	12:13:54
2	No, this is all transaction language.	12:14:27
3	I can't find it right now. Which is really	12:14:54
4	strange because we went over the references to be	12:14:57
5	correct, quite a few times.	12:15:02
6	Q. I just double checked, you also	12:15:10
7	cite the page 32 in the declaration for the '873	12:15:13
8	Patent.	12:15:18
9	A. Then it would be just consistent.	12:15:18
10	Q. So that's why if you need to take	12:15:21
11	your time to find it, you know, I wanted to make	12:15:24
12	sure we understood what you're referring to when	12:15:27
13	you cite to the address and bus command	12:15:32
14	information during the address phase and the PCI	12:15:40
15	data and byte enables during the data phase. So	12:15:45
16	if you need to take time to	12:15:48
17	A. I mean I found a few places where	12:15:48
18	that is already quite obvious, but now I'm trying	12:15:50
19	to see anywhere near page 32 because the	12:15:53
20	references should be right.	12:16:01
21	This is all about transaction ordering	12:16:46
22	which is at a higher level of bus protocol.	12:16:48
23	I would like to review this but I can give you	12:17:00
24	here another example where this is very clearly	12:17:05
25	stated, so that you have it.	12:17:09

1	Q. Where are you looking at?	12:17:10
2	A. It may not be the best example for	12:17:12
3	a citation. Page 36, which is an example of	12:17:13
4	a read transaction, 37 a write transaction. And	12:17:19
5	there you see basically the major required	12:17:26
6	functionality and signals referring to	12:17:30
7	Figure 3-1, Basic Read Operation. A PCI	12:17:40
8	transaction is always initiated by the first	12:17:43
9	clock state with frame being low, the upper	12:17:47
10	signal trace. And I should say PCI is what is	12:17:52
11	called a synchronous bus, all signals are with	12:17:55
12	Q. Can you say that again? I didn't	12:17:58
13	understand it. A what?	12:17:59
14	A. Synchronous bus.	12:18:04
15	Q. Synchronous bus, okay. My	12:18:06
16	apologies, you said it just fine, I just couldn't	12:18:06
17	pick it up. A synchronous bus, okay.	12:18:08
18	A. As compared to an asynchronous bus	12:18:10
19	which is VME.	12:18:15
20	That means basically only the signal	12:18:15
21	level we like to call it state at the	12:18:19
22	rising edge of the clock signal is relevant;	12:18:21
23	anything in between doesn't matter. Which means	12:18:25
24	you can basically take the bus state wherever	12:18:28
25	these dashed lines are or dotted lines are, the	12:18:32

1	vertical lines, and say this is a state. So	12:18:35
2	state number 1, clock number 2, frame low, always	12:18:39
3	defines the beginning of the transaction. And	12:18:44
4	the first clock of every PCI transaction has to	12:18:47
5	be the address and command. And you see that	12:18:51
6	with "AD" labeled as "address". PCI is to save	12:18:54
7	pins, what is called a multiplexed address data	12:19:02
8	bus, meaning it uses the same signal pins for	12:19:07
9	address and data information, depending on the	12:19:11
10	state of the bus. So, basically and, I mean,	12:19:14
11	this is obvious to do it like that, the first	12:19:18
12	clock says, "What does the master want to do and	12:19:21
13	where? Where is the address? What is the	12:19:25
14	command?"	12:19:27
15	I will skip the initiator and target	12:19:29
16	ready signals because they're only for flow	12:19:33
17	control.	12:19:35
18	The device selected signal is there to	12:19:36
19	enable the selected device to say, "I'm there".	12:19:38
20	The reason being it may take a long time for	12:19:46
21	a device to answer and the bus master has to be	12:19:48
22	able to disentangle the slow device from a not	12:19:52
23	existing device, which is important in case of	12:19:57
24	the automatic configuration functionality, these	12:19:58
25	whole configuration cycles.	12:20:02

1	The bus commands are nicely outlined,	12:20:03
2	and this figure I even posted in my deposition.	12:20:05
3	It's now, where are we also here in the	12:20:13
4	specification, of course, which is page I just	12:20:16
5	saw it. Here we are, page 21, right? It's	12:20:29
6	a 4-bit field, so you have 16 commands, all 16,	12:20:37
7	or mostly all 16 are defined, which gives you the	12:20:43
8	set of transactions available.	12:20:49
9	After the address phase, as it's been	12:20:52
10	called, there is an arbitrary number of data	12:20:55
11	phases, the length is only limited by some	12:20:59
12	environmental configuration, which is not	12:21:03
13	specified here, a PCI transaction must not exceed	12:21:06
14	a certain length so that nobody can block the bus	12:21:09
15	for too long. And then every time target and	12:21:12
16	initiator simultaneously say "I'm ready", data is	12:21:16
17	exchanged, as you can see from this diagram.	12:21:20
18	And that is valid for basically every	12:21:22
19	transaction although they have different meanings	12:21:25
20	and different flavors. So a configuration	12:21:27
21	transaction still would have the appropriate	12:21:30
22	command byte enables but a couple of details	12:21:32
23	would be different. And, for instance, if there	12:21:35
24	is a read multiple, these cache line type	12:21:39
25	transactions, then there is an indication as to	12:21:43

1	how many words are exchanged and so forth.	12:21:45
2	But this is basically the context which	12:21:47
3	needs to be there for a PCI transaction to be	12:21:52
4	complete. Write transaction is same thing,	12:21:54
5	except and this is why these are different	12:21:57
6	diagrams the data flow is different. We can	12:21:59
7	see nicely from Figure 3-2 that the address phase	12:22:01
8	is immediately followed by a data phase, which is	12:22:07
9	obviously making sense because if somebody wants	12:22:10
10	to write, this is then the master. The	12:22:13
11	initiator, as it's called in PCI, would have to	12:22:15
12	have the data to write otherwise it wouldn't want	12:22:18
13	to write, so it can submit the data immediately	12:22:20
14	on to the bus.	12:22:23
15	In case of a read transaction, the	12:22:24
16	target would have to notice, "Ah, I'm the one	12:22:26
17	being addressed", but then it has to access its	12:22:30
18	local resources to find that data to respond to	12:22:33
19	which is obviously not going to happen within a	12:22:36
20	clock. It cannot be. And there is an additional	12:22:39
21	requirement, there is a minimum of one clock	12:22:42
22	which is shown by these nice little arrows here,	12:22:44
23	which is called a bus turnaround cycle, because	12:22:47
24	here we have first the master driving the bus,	12:22:49
25	then data comes back to the master, so the master	12:22:52

1	has to release the bus, and the slave, the	12:22:55
2	responding device, has to drive the data signals	12:22:57
3	now. And in order to avoid race conditions where	12:23:00
4	both drive simultaneously, which is electrically	12:23:05
5	really bad, basically a short circuit, there is	12:23:10
6	this turnaround cycle.	12:23:11
7	Q. Okay, yeah, that was a lot of	12:23:15
8	testimony there, so just so we break it down	12:23:16
9	a little bit.	12:23:19
10	So you get the idea that you have to	12:23:19
11	have address and data phase and the address phase	12:23:21
12	has to include the address and bus command and	12:23:28
13	the data phase has to include the data and byte	12:23:31
14	enables from reading the specification as	12:23:32
15	a whole, in particular looking at the command	12:23:36
16	definitions, and then the explanation of how each	12:23:41
17	transaction works in this specification, right?	12:23:44
18	A. Yeah, and I think we should	12:23:46
19	probably see whether we can find a nicer	12:23:48
20	reference here because I couldn't find it, or if	12:23:51
21	I overlooked something I can point you to it	12:23:56
22	tomorrow.	12:23:58
23	Q. It's more of a summary rather than	12:23:58
24	a whole bunch of pages to read through?	12:24:00
25	A. Yeah, but, again, it's a standard.	12:24:02

1	So unfortunately these standards tend to be long	12:24:07
2	and bulky.	12:24:10
3	Q. So let me ask you something else	12:24:11
4	about what you did when you were looking at this.	12:24:13
5	If the northbridge is able to send this	12:24:17
6	information about any of these transactions, you	12:24:22
7	said there were 16, is that all that's necessary	12:24:26
8	in your mind or does this claim require that the	12:24:29
9	northbridge be able to communicate the address	12:24:33
10	and data phases of all of the different types of	12:24:37
11	PCI bus transactions laid out in this PCI	12:24:40
12	specification?	12:24:42
13	A. And which part of the document are	12:24:45
14	we now looking at, just to be clear?	12:24:47
15	Q. Which document? The declaration?	12:24:49
16	Same paragraph, 114, you say:	12:24:52
17	"[The claims] require the address and	12:24:55
18	data phases of a PCI bus transaction."	12:24:58
19	So can that be any of the 16 PCI bus	12:25:02
20	transactions or does it require that you be able	12:25:06
21	to do that for all 16?	12:25:08
22	A. Yes. For example	12:25:11
23	Q. So that what	12:25:15
24	A if you do away with the PCI	12:25:17
25	configuration you will never get to a normal	12:25:19

1	memory read or write because you can't configure	12:25:24
2	the system and it's useless. So you have to be	12:25:26
3	able to a few of them are optional, but those	12:25:30
4	required and these are configuration I/O on	12:25:34
5	memory read and write they have to be there	12:25:38
6	for the system to function.	12:25:41
7	Q. So which ones are mandatory?	12:25:43
8	A. Certainly configuration, memory	12:25:50
9	read and write. I believe also I/O. It's stated	12:25:53
10	in here somewhere. I believe that dual address	12:25:57
11	cycle is optional and only required in systems	12:26:17
12	which do 64-bit addressing in a 32-bit system.	12:26:07
13	Most of them are required.	12:26:13
14	Q. Memory read and memory write	12:26:18
15	required, right?	12:26:20
16	A. Certainly.	12:26:21
17	Q. And then you say configuration	12:26:22
18	read and configuration read are required?	12:26:24
19	A. Absolutely essential. These are	12:26:27
20	the first transactions ever done in PCI,	12:26:29
21	otherwise it won't work.	12:26:31
22	Q. What about the very first one,	12:26:32
23	interrupt acknowledge?	12:26:35
24	A. An I/O, an external device without	12:26:39
25	interrupt, will require the CPU to pull the	12:26:43

1	device, which is highly inefficient, so required.	12:26:45
2	Q. Yes, what's special cycle?	12:26:48
3	A. That I'm not sure at the moment.	12:26:54
4	Let me have a quick look. Possibly required,	12:26:56
5	possibly not; that I don't know off the top of my	12:27:00
6	head. There is a list of transactions being	12:27:02
7	outlined in here and this should also say. I	12:27:07
8	don't remember ever using it, 372, I've designed	12:27:33
9	so many pieces to play with myself. This is	12:27:45
10	a broadcast command. It doesn't say that it is	12:28:02
11	optional, so it is required. At least I don't	12:28:07
12	see that it claims it to be optional.	12:28:11
13	Q. And then there's a bunch of	12:28:15
14	reserved ones. But then you skip down to 1100	12:28:16
15	memory read multiple, is that required or	12:28:22
16	optional?	12:28:25
17	A. It's not saying optional, so it's	12:28:40
18	mandatory.	12:28:42
19	Q. And then you say dual address	12:28:43
20	cycle is optional; is that correct?	12:28:46
21	A. I believe so. Let me just verify:	12:28:48
22	" is used to transfer 64-bit address	12:28:50
23	to devices that support 64-bit addressing when	12:28:53
24	the address is not in the low 4 [gigabyte]	12:28:54
25	address space. Targets that support only 32-bit	12:28:59

1	addresses must treat this command as reserved and	12:29:02
2	not respond to the current transaction in any	12:29:05
3	way."	12:29:08
4	So this is kind of a hybrid of	12:29:09
5	mandatory; it doesn't have to be supported but	12:29:12
6	then there is a defined reaction to it.	12:29:16
7	Q. And then the next memory read	12:29:19
8	line, is that optional or mandatory?	12:29:22
9	A. It doesn't say optional so it's	12:29:36
10	required.	12:29:38
11	Q. And then finally memory write and	12:29:38
12	invalidate?	12:29:45
13	A. This is both. Cache semantics;	12:29:47
14	both don't say it is optional, so mandatory. So	12:29:55
15	basically most of it is mandatory, as I expected.	12:29:59
16	Q. So, go back to claim 24, there's	12:30:03
17	a different, slightly different phrase earlier in	12:30:19
18	the claim in the inserting step, it says that	12:30:23
19	the:	12:30:23
20	" unidirectional serial channels	12:30:31
21	that transmit encoded data of Peripheral	12:30:34
22	Component Interconnect (PCI) bus transactions in	12:30:39
23	opposite directions"	12:30:43
24	Is it your understanding and the	12:30:48
25	understanding that you applied in your analysis	12:30:50

1	of encoded data of peripheral component	12:30:52
2	interconnection bus transaction means an encoded	12:30:57
3	PCI bus transaction that includes the address and	12:31:03
4	data phases which includes the PCI address and	12:31:05
5	bus command information during the address phase	12:31:09
6	and the PCI data and byte enables during the data	12:31:11
7	phase?	12:31:15
8	MR. DAVIS: Objection; form.	12:31:16
9	THE WITNESS: You're referring to	12:31:29
10	saying is the word "data" to be interpreted in	12:31:31
11	the strictest sense of it just being data or data	12:31:35
12	in the sense of everything containing the	12:31:38
13	transaction? Did I understand the question	12:31:42
14	correctly?	12:31:46
15	BY MR. BUROKER:	12:31:47
16	Q. Well, right, is there a difference	12:31:47
17	in your mind in terms of your analysis between	12:31:49
18	data of PCI bus transaction versus, later in the	12:31:53
19	claim, address and data bits of PCI bus	12:31:58
20	transaction?	12:32:03
21	MR. DAVIS: Objection; form.	12:32:04
22	THE WITNESS: I notice that there is	12:32:08
23	a certain amount of redundancy in these claims.	12:32:09
24	Here I would say it means the encoded data as	12:32:16
25	data phases of the PCI transaction, but later	12:32:22

1	it's more detailed further in to include the	12:32:25
2	addresses as well.	12:32:35
3	BY MR. BUROKER:	12:32:38
4	Q. Right, so you would read the	12:32:38
5	"data" here as referring only to the data phase	12:32:45
6	of the PCI bus transaction?	12:32:49
7	A. I would say so. Yes.	12:33:02
8	Q. Okay, and is that because the word	12:33:05
9	"address", is not explicitly included?	12:33:07
10	A. Yes.	12:33:12
11	Q. Okay. But earlier the command	12:33:12
12	information was not explicitly included in the	12:33:18
13	phrase "address and data bits of PCI bus	12:33:21
14	transaction" and I think you said that you had to	12:33:24
15	transmit the command information done in that	12:33:28
16	<pre>claim; is that correct?</pre>	12:33:31
17	A. I remember that. For it to make	12:33:32
18	sense it has to include that, yeah.	12:33:34
19	Q. And so in the first instance for	12:33:37
20	it to make sense you don't have to send the	12:33:40
21	address information or the command information in	12:33:42
22	the "transmit encoded data of PCI bus	12:33:47
23	transaction" clause?	12:33:52
24	A. I notice you're trying to	12:33:54
25	construct a contradiction here, yeah.	12:33:56

1	Q. I'm not trying to do anything, I'm	12:33:58
2	asking you questions. It's your understanding	12:34:00
3	that you applied in your analysis.	12:34:06
4	A. Let me just	12:34:14
5	MR. DAVIS: I object to form on the	12:34:25
6	last question.	12:34:26
7	THE WITNESS: Well one claim says	12:34:29
8	"address and data bits of PCI bus transaction"	12:34:40
9	but always referring to PCI bus transactions and	12:34:44
10	up here it says "data of PCI bus transaction", it	12:34:48
11	says "encoded data".	12:34:58
12	BY MR. BUROKER:	12:35:12
13	Q. So let me just make it a simpler	12:35:12
14	question. As you applied claim 24, what did you	12:35:14
15	understand the phrase "data of PCI bus	12:35:23
16	transaction" to be?	12:35:27
17	A. I always saw this in the context	12:35:32
18	of the PCI transaction, bus transaction.	12:35:34
19	Q. Meaning that it was the data phase	12:35:38
20	of the PCI bus transaction?	12:35:39
21	A. Yeah. Let me rethink this.	12:35:47
22	Because in both cases, whether we are talking	12:36:06
23	about the lower part of the claim or the upper	12:36:09
24	part of the claim, there has to be the PCI	12:36:11
25	transaction information in there otherwise this	12:36:16

1	sentence wouldn't make much sense.	12:36:22
2	Q. So there are other asserted	12:36:25
3	claims, so claim 31 of the same patent doesn't	12:36:29
4	have the "encoded data" language, but it does	12:36:36
5	have the "address and data bits of PCI bus	12:36:40
6	transaction in serial form". Do you see that?	12:36:43
7	A. Yeah.	12:36:45
8	Q. Okay. And then claim 54 of the	12:36:46
9	'873 Patent which is the other asserted claim,	12:36:51
10	that's the other one you've got there in the	12:36:54
11	low voltage differential signal channel element	12:37:09
12	it uses the phrase:	12:37:13
13	" communicating an encoded serial	12:37:18
14	bit stream of PCI bus transaction."	12:37:21
15	Do you see that?	12:37:23
16	A. Yes.	12:37:24
17	Q. Okay. So, what do you understand	12:37:25
18	the serial bit stream of PCI bus transaction to	12:37:30
19	be? And which interpretation did you apply in	12:37:33
20	your analysis?	12:37:39
21	A. We're referring to a PCI bus	12:37:49
22	transaction, so the information which PCI bus	12:37:53
23	transaction is ongoing, what state it is at any	12:37:58
24	particular time has to be conveyed, and it is	12:38:01
25	being encoded and submitted as a serial bit	12:38:03

1	stream. So, whatever constitutes to a PCI bus	12:38:07
2	transaction, the relevant signals and we went	12:38:13
3	through it would have to be encoded in serial	12:38:18
4	form.	12:38:24
5	Q. So the whole PCI bus transaction	12:38:25
6	including any command information or byte	12:38:29
7	enables, including the address and data, that	12:38:35
8	whole thing would have to be encoded in serial	12:38:37
9	form?	12:38:42
10	A. Yes.	12:38:45
11	MR. BUROKER: Why don't we take a break	12:39:08
12	for lunch?	12:39:09
13	(Lunch recess taken 12:39 p.m 1:26 p.m.)	12:39:10
14	BY MR. BUROKER:	01:26:31
15	Q. Welcome back. I should have said	01:26:32
16	this at the beginning, but you did not talk about	01:26:36
17	the substance of your testimony with your counsel	01:26:38
18	at the lunch break, did you?	01:26:41
19	A. (The witness shook his head.)	01:26:44
20	Q. Yeah, great. That was a "no",	01:26:44
21	correct?	01:26:45
22	A. This is an affirmative.	01:26:46
23	Q. That you did not?	01:26:49
24	A. I did not.	01:26:52
25	Q. I apologize for the negative	01:26:53

1	question.	01:26:55
2	A. That's fine, don't worry. I did	01:26:56
3	not think I should.	01:26:58
4	Q. I have a question going back to	01:26:59
5	the PCI specification document. You were looking	01:27:02
6	I believe at page 36 at the read transaction as	01:27:04
7	an example of a transaction.	01:27:06
8	MR. DAVIS: Are you pointing at page 36	01:27:21
9	of the document?	01:27:23
10	MR. BUROKER: Oh, I'm sorry 36 of the	01:27:25
11	document, which is page 52 of the exhibit. It's	01:27:27
12	the 3.3.1 Read Transaction section.	01:27:30
13	A. Okay, this the one.	01:27:56
14	Q. Okay, so we were looking at this	01:27:58
15	earlier this morning, correct?	01:28:01
16	A. Yes.	01:28:02
17	Q. Are some of the elements along the	01:28:10
18	left-hand side called control lines in the PCI	01:28:11
19	specification?	01:28:14
20	A. I would consider them as such,	01:28:21
21	whether they are explicitly called control	01:28:23
22	signals I would have to check. But basically in	01:28:26
23	bus terminology you have the address, the data	01:28:33
24	and then additional corollary signals which	01:28:38
25	basically define what's going on, right? And	01:28:42

1	those constitute, in this case, the combined byte	01:28:44
2	enables, then the initiator ready, target	01:28:49
3	ready IRDY and TRDY which are basically	01:28:53
4	used for the flow control, and the device select	01:28:58
5	which is used for enabling the device to claim	01:29:01
6	its existence in the bus.	01:29:04
7	Q. What is the "frame#" what is that?	01:29:05
8	A. And frame, of course, excuse me.	01:29:09
9	The frame. The frame signal is there to define	01:29:10
10	the length of the transaction. This is a very	01:29:14
11	fundamental thing because, unlike in other cases,	01:29:17
12	in particular typically in networks, where the	01:29:21
13	length of the packet is basically submitted as	01:29:24
14	one of the very first words in the head of the	01:29:27
15	packet saying, "This is it" and, "This is how	01:29:29
16	long it will be." In PCI this doesn't exist. So	01:29:31
17	a target being connected has no way of knowing	01:29:35
18	how long this transaction will end up being,	01:29:37
19	right? It will only know here is an address and	01:29:41
20	here is a command, what is going to happen? And	01:29:44
21	the length of the transaction is determined by	01:29:46
22	the length the frame signal is asserted and if	01:29:48
23	you refer, for instance, to column 8, clock cycle	01:29:52
24	8, you see that there is one last data transfer	01:29:56
25	when frame is already high. This is basically	01:30:00

1	an efficiency thing which says since you have to	01:30:03
2	de-assert, make invalid the frame signal at the	01:30:09
3	end of the cycle to enable the next cycle, the	01:30:12
4	idea was to use that mandatory state for another	01:30:17
5	data phase in order not to have a dead state in	01:30:22
6	the bus protocol.	01:30:25
7	Q. Okay. So in a PCI bus are there	01:30:26
8	separate lines for frame number, IRDY, TRDY,	01:30:37
9	DEVSEL?	01:30:48
10	A. Yes.	01:30:48
11	Q. Okay. So of the 37 lines of a PCI	01:30:49
12	bus, those take up five of the bits; is that	01:30:53
13	correct? Or five of the lines I'm sorry.	01:31:01
14	A. If the sum is 37, I'm not	01:31:03
15	100 percent sure. But if you refer to Figure 2-1	01:31:05
16	on page 7 of the same document they are nicely	01:31:08
17	outlined. So, for example, one signal which is	01:31:11
18	also always part of the game which is not shown	01:31:11
19	here	01:31:11
20	Q. Sorry, did you say Figure 2-1?	01:31:11
21	A. Figure 2-1. The PCI pin list.	01:31:11
22	Q. Which page is that on?	01:31:31
23	A. Page 7 or 23.	01:31:31
24	So there is also the parity signal which	01:31:36
25	is used for signal integrity and then you see	01:31:38

1	here it's called the control signals, frame,	01:31:41
2	target ready, initiator ready. There is in	01:31:47
3	addition the stop signal which is not disclosed	01:31:53
4	in this diagram, which enables a device to say,	01:31:55
5	"Terminate the transaction, no point going	01:31:59
6	further, illegal address", something like that.	01:32:01
7	So there are other transactions showing that in	01:32:04
8	this spec and then device select and ID select.	01:32:08
9	Q. Yeah, I said 37 but I think it	01:32:14
10	says at the top of page 7, 47 pins not 37, right?	01:32:16
11	"The PCI interface requires a minimum	01:32:18
12	of 47 pins for a target-only device and 49 pins	01:32:20
13	for a master to handle data in addressing,	01:32:24
14	interface control, arbitration and system	01:32:28
15	functions."	01:32:30
16	Correct?	01:32:31
17	A. 37 seemed a bit low to me, yeah.	01:32:31
18	Q. Do these control lines, such as	01:32:35
19	frame, target ready, and so forth, are they part	01:32:42
20	of the PCI bus transaction as you understand that	01:32:47
21	term in the claims of the patent?	01:32:50
22	MR. DAVIS: Objection; form.	01:32:58
23	BY MR. BUROKER:	01:32:59
24	Q. So, you know, earlier we were	01:32:59
25	talking about what your understanding of the term	01:33:00

1	"PCI bus transaction", looking at paragraph 114,	01:33:03
2	for example, of your declaration, and you stated	01:33:06
3	claims require address and data phases of a PCI	01:33:10
4	bus transaction, et cetera. Are these control	01:33:17
5	lines also part of what the claims require as	01:33:19
6	a PCI bus transaction?	01:33:26
7	A. Since they are required to define	01:33:27
8	what is going on on the bus at any point in time,	01:33:30
9	the answer is yes. They define the PCI	01:33:34
10	transaction. If you, for example, would remove	01:33:37
11	from one byte enable you have no way of knowing	01:33:41
12	whether we are reading, writing, or what other	01:33:46
13	functionality is to be executed. If you remove	01:33:49
14	any of the flow control signals, you cannot steer	01:33:51
15	the fact if a device is not immediately ready,	01:33:57
16	which happens a lot. So they would have to be	01:33:59
17	they define the transaction, so have to be there.	01:34:05
18	Q. Okay. Looking at claim 24 as	01:34:09
19	an example again.	01:34:14
20	A. Just wait, wait. And we are	01:34:20
21	talking now '873?	01:34:21
22	Q. No, '814 Patent, claim 24.	01:34:36
23	The complete phrase that we were looking	01:34:36
24	at talks about communicating address and data	01:34:38
25	bits of PCI bus transaction in serial form. Do	01:34:47

1	you see that?	01:34:49
2	A. Yes.	01:34:49
3	Q. PCI bus transactions are not	01:34:54
4	naturally in a serial form, correct?	01:34:56
5	A. They are not defined in a serial	01:34:58
6	form in this document, correct.	01:34:59
7	Q. So if you take the transaction and	01:35:10
8	transform it into a serial format, is the result	01:35:13
9	still a PCI bus transaction?	01:35:16
10	MR. DAVIS: Objection; form.	01:35:20
11	(Brief pause to re-establish realtime connections.)	01:38:22
12	BY MR. BUROKER:	01:38:22
13	Q. Since we had a little bit of	01:38:23
14	a technical issue, I'll just ask a new question.	01:38:24
15	The phrase is:	01:38:27
16	" to communicate [the] PCI bus	01:38:28
17	transaction in serial form"	01:38:31
18	What does it mean to you to communicate	01:38:35
19	a PCI bus transaction in serial form?	01:38:38
20	MR. DAVIS: Objection; form.	01:38:42
21	BY MR. BUROKER:	01:38:46
22	Q. Well in actual fact let me ask	01:38:47
23	a different question.	01:38:49
24	So the full language, and I'll give it	01:38:49
25	to you, is:	01:38:51

1	" to communicate address and data	01:38:52
2	bits of PCI bus transaction in serial form"	01:38:54
3	What does the phrase "in serial form"	01:38:56
4	in that phrase mean?	01:39:01
5	A. I mean, I defined even in	01:39:04
6	particular this serial transmission here, and,	01:39:08
7	let me just see, '814, there were a few terms	01:39:18
8	which I believe have been defined, now I just	01:39:21
9	have to see that I find it real quick, serial	01:39:24
10	communication, page 28 of this document. And	01:39:27
11	although I am quite sure I remember off the top	01:39:33
12	of my head, I'd rather refer to it. We say here:	01:39:39
13	"Serial communication protocols"	01:39:44
14	and I was instructed to speak really	01:39:48
15	slow when I read because I was not doing this	01:39:50
16	" send bits of information one after	01:39:53
17	another on one or more lines that are used to	01:39:54
18	make up words. A communication scheme is said to	01:39:57
19	be serial if the information sent over the serial	01:40:05
20	lines has more bits in a word than there are	01:40:07
21	physical lines to transmit those bits."	01:40:10
22	And then there is more details, but I	01:40:12
23	think this is maybe already good enough for this.	01:40:15
24	So that means the information defining	01:40:19
25	a PCI transaction is sent over a number of	01:40:23

1	signals which are obviously less than what we	01:40:28
2	have here. The corollary to that technically	01:40:32
3	would mean it would have to be at a higher rate	01:40:37
4	in order to keep up.	01:40:40
5	Q. And while that information is	01:40:42
6	being transmitted over the serial line, is it	01:40:44
7	still a PCI bus transaction?	01:40:48
8	MR. DAVIS: Objection to form.	01:40:54
9	THE WITNESS: Here I would stick to the	01:40:59
10	specification and one of the functionalities and	01:41:03
11	features of a specification requires that	01:41:07
12	compliant devices can communicate with each other	01:41:09
13	directly. So with a serialized version of this,	01:41:13
14	although the entire information may be there but	01:41:19
15	in a different form, one could not connect	01:41:21
16	directly a PCI compliant device for it to work,	01:41:24
17	it would have to be reconverted into the ordinary	01:41:28
18	or defined PCI format for this to work.	01:41:31
19	BY MR. BUROKER:	01:41:35
20	Q. So the claims, in your reading,	01:41:35
21	contemplate some sort of transformation of the	01:41:38
22	PCI bus transaction into a format that is	01:41:43
23	serially transmitted and then, on the other end,	01:41:48
24	it would be converted back into PCI bus	01:41:53
25	transaction format?	01:41:58

1	MR. DAVIS: Objection; form.	01:41:58
2	THE WITNESS: The patent text outlines	01:42:01
3	this in great detail, and this is the context in	01:42:04
4	which I would read this claim. Because it has to	01:42:06
5	be seen in the context of the patent. So yes.	01:42:12
6	BY MR. BUROKER:	01:42:17
7	Q. If you add information to the PCI	01:42:44
8	bus transaction is that resulting set of data	01:42:46
9	still a PCI bus transaction?	01:42:54
10	MR. DAVIS: Objection; form.	01:42:58
11	THE WITNESS: Can you be more specific?	01:43:01
12	BY MR. BUROKER:	01:43:03
13	Q. Right, so if there's 47 lines in	01:43:03
14	a PCI bus transaction, if you add five additional	01:43:06
15	lines of information for whatever reason, is the	01:43:12
16	resulting 55-bit piece of information still a PCI	01:43:15
17	bus transaction?	01:43:21
18	MR. DAVIS: Objection; form.	01:43:23
19	THE WITNESS: The game about standards	01:43:28
20	is quite clear: what is in the standard is what	01:43:29
21	it is, no more no less. So answering your	01:43:33
22	question, I say what you have now is some	01:43:37
23	superset of a PCI transaction, which would be	01:43:42
24	part of something else. That additional	01:43:44
25	information has no meaning with respect to the	01:43:47

1	PCI transaction.	01:43:49
2	BY MR. BUROKER:	01:43:53
3	Q. Right, so let me just refer you to	01:43:53
4	paragraph 80 of your declaration. You discuss	01:43:57
5	some of the figures from the '814 Patent, right?	01:44:09
6	And 80 is fairly long with lots of figures, so if	01:44:15
7	you need to read it that's fine.	01:44:18
8	In there you note that the inventor in	01:44:20
9	these figures contemplates adding something he	01:44:23
10	called bus status bits; is that correct?	01:44:26
11	A. Yeah.	01:44:30
12	Q. Okay. And then the PCI bus	01:44:32
13	transaction plus these bus status bits are	01:44:37
14	encoded into a form that are then set serially	01:44:43
15	over a serial bus. Is that your understanding of	01:44:48
16	what's shown in Figures 13, 14 and 17?	01:44:51
17	A. Let me just see. 14 I can see.	01:44:58
18	Are you talking about the figures in the claim	01:45:11
19	13, 14, 17? I'm sorry.	01:45:15
20	Q. No, the figures in the patent.	01:45:16
21	A. 17 and 14, but where is 13?	01:45:20
22	There's one. Do I have the wrong one? You're	01:45:32
23	talking '814, right?	01:45:34
24	Q. Right, paragraph 80. Within	01:45:36
25	paragraph 80, you have included	01:45:40

1	A. This diagram, yes, 17.	01:45:43
2	Q Figures 17, 13 and 14 out of	01:45:45
3	the '814 Patent.	01:45:51
4	A. Oh, sorry, I see this. I took the	01:45:51
5	whole thing for Figure 14 and I overlooked that	01:45:53
6	there is a Figure 13 on top of it. Yes, this is	01:45:56
7	correct.	01:45:58
8	Q. Okay, so you're looking at the	01:45:58
9	right thing?	01:46:00
10	A. Yes.	01:46:00
11	Q. And then you point to in your	01:46:00
12	text, you say that what is the label with the red	01:46:03
13	box let's see what number it is 5 are what	01:46:06
14	you call bus status bits. Do you see that?	01:46:19
15	A. Yeah.	01:46:23
16	Q. And that's not part of a typical	01:46:23
17	PCI bus transaction, these bus status bits,	01:46:26
18	right?	01:46:28
19	A. Correct. They would have to be in	01:46:29
20	the figure we just looked at on page 7 for it to	01:46:32
21	be part of the standard.	01:46:36
22	Q. So my question to you is then is	01:46:43
23	what is shown in Figure 13 and 14 a PCI bus	01:46:47
24	transaction in serial form?	01:46:57
25	A. Now, I'm	01:47:04

1	MR. DAVIS: Objection to form. Sorry,	01:47:04
2	I didn't mean to interrupt.	01:47:06
3	THE WITNESS: If you look at page 49,	01:47:09
4	it says the bus status bits:	01:47:17
5	" BS0 [through] BS3 in Figures 13	01:47:21
6	and 14 are 'bus status' bits added by the	01:47:24
7	inventor to facilitate serialized communication	01:47:32
8	and form 10 bit packets, which may include	01:47:38
9	PCI-related information like the FRAME	01:47:42
10	[initiator and target ready] signals."	01:47:47
11	So basically they put it there and have	01:47:49
12	given it just a different name, but this is	01:47:57
13	basically the placeholder for these PCI-related	01:48:01
14	signals. But they may have different meanings	01:48:04
15	depending on whether or not the signal goes	01:48:08
16	initiator to target or target to initiator	01:48:11
17	because these are unidirectional signals.	01:48:13
18	So the conclusion to say these are not	01:48:18
19	PCI signals is not exactly correct. These are	01:48:20
20	PCI signals, it's just a different name for	01:48:23
21	a kind of a placeholder, if you want to code	01:48:28
22	them.	01:48:30
23	BY MR. BUROKER:	01:48:31
24	Q. So they've taken the PCI-required	01:48:31
25	signals and created placeholders for them. Was	01:48:35

1	the result of that still PCI bus transaction or	01:48:40
2	is it something different?	01:48:43
3	MR. DAVIS: Objection; form.	01:48:45
4	THE WITNESS: I mean, that discussion	01:48:48
5	we had before, this is a serialized version of	01:48:49
6	a PCI bus transaction which has to include	01:48:54
7	everything necessary to define that transaction	01:48:55
8	accurately, but this particular encoding signals	01:48:58
9	on wires sequences of bits on those signals is	01:49:04
10	not, in the strict sense of the specification,	01:49:11
11	a PCI bus anymore, but it has everything in it to	01:49:14
12	very easily recreate it, which is an important	01:49:19
13	thing. One to one create it with all details in	01:49:21
14	it. Right? So, for example, also the definition	01:49:27
15	what is the sequence of address bits which go on	01:49:36
16	to the individual signal lines because we have a	01:49:39
17	tenfold increase in clock rate enabling to get	01:49:44
18	the number of parallel signals appropriately	01:49:47
19	down.	01:49:52
20	BY MR. BUROKER:	01:49:53
21	Q. So, in summary, is it your	01:49:53
22	understanding that the phrase we looked at in	01:49:57
23	claim 24 requires that what is communicated are	01:50:00
24	all of the pieces of information needed to	01:50:05
25	recreate the PCI bus transaction on the other end	01:50:08

1	of the serial transmission?	01:50:13
2	A. Right, the PC	01:50:15
3	MR. DAVIS: Just pause and let me	01:50:18
4	object in between. Objection; form.	01:50:19
5	BY MR. BUROKER:	01:50:23
6	Q. You can answer.	01:50:23
7	A. I shouldn't give quick answers so	01:50:25
8	that we don't have these collisions.	01:50:27
9	Q. Do you need her to read back?	01:50:27
10	A. Yeah, I apologize, could you?	01:50:51
11	(The record was read back.)	01:50:51
12	MR. DAVIS: Objection; form.	01:50:51
13	THE WITNESS: Again, and I confirm that	01:50:53
14	and wish to add, of course, the PCI bus	01:50:56
15	transaction initiated by the bus master at the	01:50:59
16	other side of this interface. It's not any PCI	01:51:02
17	bus transaction, it's the particular one on the	01:51:07
18	other side of the interface.	01:51:10
19	BY MR. BUROKER:	01:51:23
20	Q. So, the second term that was	01:51:25
21	discussed is the word "encoded" and it's	01:51:29
22	paragraph 116 where that section starts and goes	01:51:34
23	through 120.	01:51:39
24	So in paragraph 116 you state that you	01:51:45
25	believe that the broadest reasonable	01:51:49

1	interpretation of encoded requires that it must	01:51:51
2	be reversible; is that correct?	01:51:56
3	A. That's correct.	01:52:00
4	Q. Okay. And is that language, the	01:52:01
5	reversible language, required by the IBM	01:52:08
6	technical dictionary you cite?	01:52:14
7	A. Yes.	01:52:16
8	Q. Where is that?	01:52:16
9	A. It's a bit of a complicated	01:52:33
10	language in this dictionary. Encoding well, I	01:52:35
11	mean it defines here first of all the term	01:52:43
12	"code", which is:	01:52:46
13	"A set of rules that maps the elements	01:52:47
14	of one set onto the elements of another set	01:52:50
15	The first set is the coded set and the second set	01:52:53
16	is the code element set. [The] element of [one]	01:52:56
17	code element may be related to more than one	01:52:59
18	element of the coded set <u>but the reverse is not</u>	01:53:02
19	<u>true</u> ."	01:53:05
20	That means basically you have many ways	01:53:05
21	of encoding but there's always the one-to-one	01:53:07
22	relationship. One example the famous ASCII code,	01:53:10
23	turning letters into codes. There is	01:53:15
24	a one-to-one relationship for every letter being	01:53:19
25	a code. For example, capital A is hexadecimal	01:53:22

1	41. And this is a one-to-one relationship.	01:53:28
2	Anything else wouldn't make sense because once	01:53:32
3	you have the code you couldn't recreate the	01:53:34
4	letter if there was an ambiguity. But there are	01:53:36
5	other codes, for example, Unicode. It turns out	01:53:39
6	ASCII code has limitations. It was invented in	01:53:42
7	America and at that time people didn't notice	01:53:47
8	that we have what we call umlaut in Germany,	01:53:50
9	accents in French, so that all doesn't exist, and	01:53:53
10	then the entire Arabian space where you have all	01:53:57
11	these different letters, so Unicode was invented.	01:54:02
12	While ASCII is a seven-bit code, every character	01:54:07
13	seven bits, Unicode is a 16-bit code, so you have	01:54:20
14	65,000 characters possible. And you have to now,	01:54:14
15	if you have a code, of course tell which is the	01:54:19
16	context, which coding rules that has been used,	01:54:22
17	but there always has to be a one-to-one	01:54:25
18	relationship. Or, in other words, there always	01:54:27
19	is a decoder for an encoder.	01:54:30
20	Q. Let me just hand to you the IBM	01:54:37
21	dictionary which was being cited here, which was	01:54:40
22	previously marked Acqis Exhibit 2024 in the '1469	01:54:46
23	IPR proceeding.	01:54:50
24	Do you recognize this set of pages out	01:54:51
25	of the IBM technical dictionary?	01:54:54

1	A. I recognize it. It's a bit bigger	01:54:56
2	than that, yeah.	01:54:58
3	Q. Yes, a little bit bigger.	01:54:59
4	So you looked at the definition of	01:55:01
5	"code" and there are 13 actual definitions under	01:55:02
6	the word "code". You cite just one. Did you	01:55:10
7	look at the others to see if they were	01:55:14
8	applicable?	01:55:17
9	A. I mean there is a lot of different	01:55:27
10	examples here, but they all fall under the same	01:55:29
11	fundamental principle I state here, so I believe	01:55:31
12	the correct answer here would be then yes, but we	01:55:34
13	can go through them to be really absolutely sure:	01:55:37
14	"A set of items, such as abbreviations,	01:55:42
15	representing the members of another set."	01:55:45
16	It's a generic form of encoding.	01:55:48
17	Q. Definition (2) doesn't explicitly	01:55:53
18	say that coding requires reversibility, does it?	01:55:59
19	A. But it's in the context of the	01:56:12
20	overall definition.	01:56:14
21	Q. So you read (2) in context of (1).	01:56:18
22	Is that what you're saying?	01:56:21
23	A. Yeah. I mean, this is all under	01:56:23
24	the section "code" anyway. And also if you use	01:56:24
25	abbreviations to represent a particular member of	01:56:35

1	another set, how much sense does it make if this	01:56:39
2	abbreviation is ambiguous?	01:56:44
3	Q. Okay. Some other terms are used	01:57:23
4	in the patent but there's no explicit section, so	01:57:26
5	I wanted to see if you could explain what you	01:57:30
6	understood those to mean. So in claim 24 of the	01:57:34
7	'814 Patent there is the phrase "northbridge"	01:57:37
8	used, we've talked about that clause a number of	01:57:46
9	times. What did you understand the phrase	01:57:48
10	"northbridge" to mean in the context of claim 24	01:57:50
11	of the '814 Patent?	01:57:53
12	A. I believe I have a drawing in here	01:57:57
13	which should outline that. In general as being	01:58:00
14	referred to as the interface device which is	01:58:05
15	interfacing the processor to the memory and some	01:58:13
16	additional I/O devices which are typically then	01:58:17
17	called "southbridge". And the term "northbridge"	01:58:20
18	basically came from the fact that usually here	01:58:22
19	is an example the processor is drawn on top	01:58:26
20	and	01:58:29
21	Q. Sorry, you need to just say what	01:58:30
22	you're referring to because there's no way to get	01:58:31
23	that on the transcript. You're looking at what	01:58:34
24	page of your declaration?	01:58:36
25	A. I'm looking at page 33 of the	01:58:38

1	declaration, which is Figure 1-4, called, "PCI	01:58:40
2	Based System Showing Implementation of a	01:58:47
3	PCI-to-PCI Bridge."	01:58:47
4	It's just one example of a computer. I	01:58:49
5	mean here you see as an example that the	01:58:53
6	northbridge functionality, in this example a chip	01:58:56
7	from Intel, basically interfaces directly to the	01:58:59
8	processor through its front side bus and on the	01:59:03
9	other side to the main memory of that processor,	01:59:08
10	here called SDRAM, to the graphics. This is	01:59:14
11	an old figure, so it still has the advanced	01:59:17
12	graphics port (AGP) and at the bottom has	01:59:20
13	S-interface with the periphery a PCI interface	01:59:24
14	where the southbridge again interfaces the PCI	01:59:27
15	also and has a large number of different, much	01:59:30
16	slower, typically much slower interfaces such as	01:59:34
17	IDE, USB, ISA bus, and so forth.	01:59:40
18	Q. And so then the term "peripheral	01:59:47
19	bridge" is used in claim 31 of the same patent.	01:59:50
20	What understanding did you give to that term?	01:59:57
21	A. Peripheral devices a typically	02:00:02
22	considered well, periphery to a computer to	02:00:07
23	a processor could be anything like a keyboard,	02:00:10
24	mouse, hard drive, network interfaces and so	02:00:17
25	force. So a peripheral bridge would be	02:00:21

1	an interface between those devices having very	02:00:23
2	many different possible standards, and the	02:00:29
3	computer, the core of the computer.	02:00:31
4	Q. So claim 31 specifically says that	02:00:37
5	the peripheral bridge is coupled to	02:00:40
6	a microprocessor unit, without an intervening PCI	02:00:44
7	bus. So, in that particular case, the peripheral	02:00:48
8	bridge would have to have a connection to the	02:00:52
9	microprocessor and no intervening peripheral bus;	02:00:56
10	is that right?	02:01:00
11	A. This is what the claim says, yes.	02:01:01
12	Q. Right. And then claim 24, going	02:01:02
13	back, the northbridge, it states, has to be	02:01:07
14	directly coupled to the microprocessor unit. Do	02:01:09
15	you see that?	02:01:14
16	A. Just not yet.	02:01:16
17	Q. In claim 24, it says the	02:01:17
18	northbridge and then it says:	02:01:20
19	"Said north bridge directly coupled to	02:01:23
20	the microprocessor unit."	02:01:25
21	A. Yes, I see, yeah, yeah.	02:01:27
22	Q. And then claim 54 of the '873	02:01:29
23	Patent I'm going to have you flip to	02:01:45
24	a different patent the last element of claim	02:01:47
25	54 is the peripheral bridge. Do you see that?	02:01:56

1	A. " directly coupled to the	02:01:59
2	processing unit."	02:02:00
3	Q. Right, so in this case the	02:02:01
4	peripheral bridge has to be directly coupled to	02:02:05
5	the processing unit, not just coupled as in claim	02:02:07
6	31 of the '814, correct?	02:02:09
7	A. It states it that way, yes.	02:02:11
8	Q. And did you use the same	02:02:13
9	understanding of the term "peripheral bridge" in	02:02:15
10	your analysis of both patents? In other words	02:02:18
11	claim 31 of the '814 and claim 54 of the '873	02:02:21
12	patent?	02:02:26
13	MR. DAVIS: Objection; form.	02:02:28
14	THE WITNESS: Peripheral bridge in 31	02:02:49
15	and, excuse me, 54 it was.	02:02:51
16	Yeah, in both cases, there is no	02:02:52
17	further limitation on the peripheral bridge, so	02:03:01
18	the definition holds.	02:03:07
19	BY MR. BUROKER:	02:03:09
20	Q. Is there any minimum set of	02:03:09
21	requirements, that you can think of, that	02:03:11
22	something has to have to be a peripheral bridge	02:03:16
23	as understood in these claims?	02:03:21
24	MR. DAVIS: Objection; form.	02:03:24
25	THE WITNESS: I am not aware of	02:03:30

1	a definition, an official definition what has to	02:03:31
2	be a peripheral bridge like what is PCI standard,	02:03:37
3	but in this context obviously the peripheral	02:03:41
4	bridge has to have an interface to the processor	02:03:48
5	and since the limitation is made clearly directly	02:03:51
6	coupled in some cases, there is obviously	02:03:55
7	different ways to do this and obviously it has to	02:03:59
8	have an interface circuitry to peripheral	02:04:01
9	devices, one or many.	02:04:08
10	BY MR. BUROKER:	02:04:26
11	Q. So we talked about this a little	02:04:26
12	bit, the word in claim 24 of the '814 Patent, the	02:04:27
13	word "communicate" is used, it says:	02:04:32
14	" the north bridge to	02:04:37
15	communicate"	02:04:38
16	and then the rest of the clause.	02:04:39
17	What's your understanding of what that verb	02:04:41
18	"communicate" means in the context of claim 24?	02:04:44
19	Let me strike that and say what do you	02:04:54
20	believe the broadest reasonable interpretation of	02:04:56
21	the term "communicate" is that you applied in	02:04:58
22	analyzing the claims versus the references in	02:05:02
23	these IPRs?	02:05:05
24	A. In this case and we're talking	02:05:13
25	now the '814 Patent, claim 24 the northbridge	02:05:14

1	which communicates, sends this information to	02:05:18
2	some recipient such that it can decode the	02:05:22
3	information appropriately or decode (sic).	02:05:26
4	Q. Do you believe communication then	02:05:28
5	is limited to transmitting and does not include	02:05:31
6	receiving?	02:05:35
7	A. I'm hesitant to answer immediately	02:05:51
8	because the claim here basically doesn't specify	02:05:53
9	who is receiving, but in general communication	02:05:56
10	makes little sense if nobody receives the	02:05:59
11	information. That is true, that is clear. It	02:06:01
12	could be seen implicitly here in the claim.	02:06:05
13	Obviously it's being received and used.	02:06:07
14	Q. But my question is whether the	02:06:12
15	northbridge if the northbridge only received	02:06:14
16	address and data bits of PCI bus transaction in	02:06:20
17	serial form, didn't transmit them, would that	02:06:23
18	element be met?	02:06:30
19	MR. DAVIS: Objection; form.	02:06:32
20	BY MR. BUROKER:	02:06:36
21	Q. You might imagine like, I know	02:06:36
22	that some of these transactions we talked about	02:06:39
23	are just one-way transactions. So if there was	02:06:43
24	a northbridge that only received a PCI bus	02:06:46
25	transaction in serial form and didn't transmit	02:06:49

1	anything in response, would it meet, in your	02:06:54
2	understanding, the requirement of this claim?	02:06:56
3	A. Now, two things. Yes, there are	02:06:59
4	communication channels but now outside of this	02:07:03
5	patent, which could be one-way, right? So, for	02:07:05
6	example, if you switch on the radio and listen to	02:07:13
7	the news there is a communication happening	02:07:16
8	between the radio broadcaster and you receiving	02:07:19
9	that message and there is no way of you talking	02:07:22
10	back. However here we have communication of	02:07:24
11	address and data bits of PCI bus transaction and	02:07:24
12	PCI bus transactions are defined here as being	02:07:33
13	reading and writing and that requires	02:07:34
14	bi-directional communication, right? Simple	02:07:39
15	example, a read transaction requires the bus	02:07:41
16	master, the initiator, to send an address to the	02:07:44
17	target, information goes out. But without data	02:07:46
18	coming back, answering that read, there is no	02:07:51
19	read transaction. So, the fact that this is	02:07:54
20	a communication of a PCI bus transaction requires	02:07:58
21	it to be bi-directional full duplex, as we say.	02:08:00
22	(The court reporter sought	02:08:00
23	clarification.)	02:08:00
24	THE WITNESS: Or a full duplex.	02:08:18
25	BY MR. BUROKER:	02:08:21

1	Q. Bi-directional, I think, right?	02:08:21
2	Sir, that's what you meant to say?	02:08:22
3	A. (The witness nodded.)	02:08:23
4	Q. Yeah, I didn't want to	02:08:25
5	A. That might be a bit of a German	02:08:25
6	accent thing.	02:08:29
7	Q. That's fine, I just want to make	02:08:30
8	sure we get a clear record.	02:08:31
9	And then in claim 31, instead of the	02:08:33
10	word "communicate", the language in another part	02:08:40
11	of the claim says "transmit". I'm sorry, no, I	02:08:45
12	meant earlier in the claim, in claim 24, if you	02:08:55
13	look up there.	02:09:00
14	A. Uh-huh.	02:09:00
15	Q. There the language was that the	02:09:02
16	console has an LVDS channel "that transmit	02:09:05
17	encoded data".	02:09:11
18	A. Yeah.	02:09:12
19	Q. So in that situation what is your	02:09:13
20	belief as to the broadest reasonable	02:09:16
21	interpretation of the word "transmit" in claim	02:09:19
22	24?	02:09:22
23	MR. DAVIS: Objection; form.	02:09:23
24	THE WITNESS: I mean we have two	02:09:29
25	unidirectional serial channels that transmit	02:09:39

1	encoded data of peripheral component interconnect	02:09:43
2	bus transactions. So every individual channel is	02:09:49
3	a one way thing but they are opposite direction,	02:09:53
4	so each of the two ones transmit their part of	02:09:57
5	the entire PCI transaction. It goes together.	02:10:02
6	BY MR. BUROKER:	02:10:02
7	Q. But the word "transmit" is	02:10:06
8	a one-way passage of data, it's just in the	02:10:11
9	context of the claim you're saying because there	02:10:17
10	are two pairs	02:10:19
11	A. Yeah.	02:10:20
12	Q that the serial channel sends	02:10:21
13	things both ways; is that correct?	02:10:22
14	A. Yes, each and every one is	02:10:24
15	a unidirectional but together it is	02:10:26
16	bi-directional again and without that a read	02:10:30
17	transaction would not be possible.	02:10:34
18	Q. So then later on in this claim,	02:10:41
19	the word "convey" is used. So if you look down	02:10:45
20	at the phrase that starts:	02:10:49
21	"The second LVDS channel"	02:10:50
22	et cetera, et cetera, et cetera.	02:10:52
23	Later on in that same clause it says:	02:10:54
24	" said second LVDS channel extending	02:10:57
25	from said north bridge to convey said address and	02:11:00

1	data bits of PCI bus transaction in serial form."	02:11:04
2	Do you see where I am?	02:11:10
3	A. Yeah.	02:11:13
4	Q. So what is the broadest reasonable	02:11:14
5	interpretation of the word "convey" in the	02:11:16
6	context of the claim that we just read?	02:11:17
7	A. This is just a different word for	02:11:30
8	the same thing. The information about the PCI	02:11:32
9	bus transaction is communicated or exchanged or	02:11:39
10	conveyed and this is, in this case, done in	02:11:48
11	serial form. I read this such that whoever	02:11:51
12	constructed that claim just used a different word	02:11:57
13	for it to be possibly a bit better readable.	02:12:00
14	Q. Okay, now looking at which patent,	02:12:11
15	54 of the '873?	02:12:15
16	A. Yes.	02:12:17
17	Q. Now I want to ask you about we	02:12:32
18	may have touched on this a bit earlier the	02:12:35
19	phrase in the second-to-last clause, there's the	02:12:38
20	low-voltage differential signal, that clause.	02:12:41
21	Later on it says:	02:12:44
22	" to transmit data in opposite	02:12:47
23	directions for communicating an"	02:12:49
24	and here's the question	02:12:52
25	" encoded serial bit stream of	02:12:54

1	(PCI) bus transaction"	02:12:56
2	Does that mean that all of the elements	02:13:01
3	of the PCI bus transaction have to be encoded,	02:13:07
4	including the address data control signals,	02:13:13
5	et cetera?	02:13:18
6	A. Whatever pertains to the PCI	02:13:18
7	transaction otherwise it wouldn't be complete,	02:13:21
8	yeah.	02:13:23
9	Q. And to your understanding of the	02:13:24
10	broadest reasonable interpretation, the encoding	02:13:27
11	must be done in such a way that it's reversible	02:13:29
12	on the receiving end; is that correct?	02:13:32
13	A. Absolutely, I mean, in particular	02:13:34
14	also if you look at this in the context of this	02:13:38
15	patent it wouldn't make much sense if this	02:13:43
16	encoding would not be reversible because then the	02:13:47
17	far end would not be able to recreate the	02:13:49
18	transaction.	02:13:51
19	Q. I'll direct you to page 91 (sic)	02:14:09
20	of your '814 declaration?	02:14:11
21	A. Yeah.	02:14:31
22	Q. You're talking about the TNet	02:14:32
23	solution which is TNet, T-N-e-t from the	02:14:41
24	Horst reference that we'll be talking about	02:14:41
25	shortly. But you say:	02:14:44

1	"The TNet solution, discussed in the	02:14:45
2	Horst reference, was not solving the same problem	02:14:48
3	as that encountered by Dr. Chu in the '814	02:14:51
4	patent."	02:14:54
5	Do you see where I'm talking about?	02:14:55
6	A. Not quite yet.	02:14:57
7	Q. The very first sentence of	02:14:59
8	paragraph 91.	02:15:00
9	A. Oh, I have page 91. That's	02:15:01
10	something else.	02:15:05
11	Q. Oh, that's not the same.	02:15:06
12	A. Yes. I'm right there.	02:15:12
13	Q. Okay. So is it your understanding	02:15:13
14	that a prior reference has to be solving the same	02:15:21
15	problem as the inventor in order to invalidate	02:15:25
16	it?	02:15:32
17	A. No, it does not.	02:15:32
18	Q. So what was the reason that you	02:15:33
19	said they're not solving the same problem?	02:15:35
20	A. Whatever has been cited as prior	02:15:41
21	art has to make sense as a functioning system if	02:15:45
22	put together and, I mean, this is just the	02:15:49
23	introductory sentence to a rather long chain of	02:15:53
24	arguments, where these things are detailed more.	02:15:57
25	So taking out of context, yes, this is not enough	02:16:03

1	to make this plain. The fundamental difference	02:16:05
2	between these two scenarios, what is described in	02:16:12
3	the patent and what is outlined in the Horst	02:16:17
4	reference is basically one is a parallel computer	02:16:20
5	system, supporting up to, I believe, a million of	02:16:24
6	nodes, where the other is something where you	02:16:26
7	have one single computer with a completely	02:16:30
8	confined context and functionality allowing to	02:16:33
9	connect an I/O subsystem or a console in a highly	02:16:38
10	efficient way. So many of the things required in	02:16:43
11	this context to be there would hinder what is	02:16:51
12	disclosed by Chu and if one would try to	02:16:57
13	introduce, to basically impose what is disclosed	02:17:00
14	by Chu on TNet it wouldn't work anymore, you have	02:17:04
15	a single address base in PCI and you cannot	02:17:07
16	possibly have that in such a distributed system.	02:17:10
17	Q. So it's not your understanding,	02:17:16
18	and you were not trying to, as part of your	02:17:18
19	invalidity analysis, determine that the claims	02:17:23
20	solved the same problem as the prior art? That	02:17:27
21	was not something that you felt like you had to	02:17:29
22	find in order for there to be invalidity, right?	02:17:31
23	Let me ask that again.	02:17:35
24	You were not operating under the	02:17:38
25	understanding that to show something is invalid,	02:17:39

1	a claim is invalid based on a reference that the	02:17:41
2	claim and the reference are addressed to the same	02:17:44
3	problem?	02:17:47
4	A. This is not a requirement, but if	02:17:50
5	you ask about the basics of the analysis, I have	02:17:51
6	that outlined, starting at page 10, right? I	02:17:58
7	mean this is the whole claim construction	02:18:02
8	business. In particular this is about	02:18:05
9	anticipation and obviousness, right? And both	02:18:08
10	principles I have applied to the best of my	02:18:13
11	knowledge. I guess the most important one is	02:18:15
12	about obviousness, right? Most of the claims	02:18:19
13	which are under discussion here are on the	02:18:25
14	obviousness issue. I mean there's quite a bit of	02:18:29
15	text which I put in, you know, hoping to make it	02:18:35
16	clear.	02:18:39
17	Q. So you just mentioned that one of	02:18:40
18	the differences with Chu and the Horst reference	02:18:43
19	had to do with addressing and you indicate that	02:18:47
20	the Horst reference uses virtual addressing; is	02:18:54
21	that correct?	02:18:57
22	A. This is correct and it is stated	02:18:58
23	in the Horst reference which means now would be	02:19:00
24	a good time	02:19:03
25	Q. Do you need a copy?	02:19:05

1	A to have it so that I can point	02:19:06
2	you to, if I can find it quickly. But it makes	02:19:08
3	a clear point, and there is also a technical	02:19:12
4	requirement for this to be the case. It's	02:19:15
5	similar in SCI.	02:19:22
6	Q. So this is Horst, which is 1009 in	02:19:25
7	'814 IPR but it is also 1011 in the '873 IPR. So	02:19:31
8	I'm giving you the copy that was marked 1009 in	02:19:38
9	the '814.	02:19:41
10	So my question I was going to ask you is	02:19:54
11	really about virtual addressing versus physical	02:19:59
12	addressing which you say that PCI devices use	02:20:03
13	physical addressing; is that correct?	02:20:08
14	A. Yes.	02:20:10
15	Q. And is it your understanding that	02:20:12
16	the claims that are at issue in these IPR	02:20:14
17	proceedings exclude virtual addressing?	02:20:18
18	MR. DAVIS: Objection; form.	02:20:22
19	THE WITNESS: I mean you now ask for	02:20:26
20	all claims?	02:20:27
21	BY MR. BUROKER:	02:20:29
22	Q. No, no, the claims in the IPR	02:20:29
23	proceedings, we can start with claim 24 in the	02:20:31
24	'814. Is there any language you were looking at	02:20:34
25	where it says virtual addressing is excluded?	02:20:38

1	A. It says always in the context of	02:20:44
2	addresses, addresses of PCI bus transaction.	02:20:51
3	Since PCI bus transactions are meant, it has to	02:20:55
4	be physical addresses. So this is basically part	02:20:59
5	of the context of it being PCI, right?	02:21:01
6	And let me maybe to have a clean	02:21:04
7	differentiation between a virtual and physical	02:21:12
8	addresses, because I'm sure we will have more of	02:21:14
9	that. The important thing is a physical address	02:21:17
10	enables to locate the particular device or the	02:21:23
11	particular word in memory unambiguously. This is	02:21:26
12	what it is. Unlike a virtual address. And since	02:21:31
13	these claims are about the physical I/O bus PCI	02:21:36
14	using physical addresses, because in here the PCI	02:21:41
15	address is used to select the device connected on	02:21:44
16	the bus, and there could be any number of devices	02:21:47
17	connected there. It has to be a physical	02:21:49
18	address. The final result of any	02:21:52
19	physical-to-virtual sorry, virtual-to-physical	02:21:55
20	address translation. I misspoke.	02:22:01
21	Q. Would you agree the claim 24	02:22:06
22	contemplates the creation of a serial form of the	02:22:13
23	PCI bus transaction?	02:22:19
24	A. I mean I would stick to the exact	02:22:41
25	claim language and, I mean, it says really	02:22:43

1	clearly:	02:22:53
2	" serial channels that transmit	02:22:55
3	encoded data of Peripheral Competent Interconnect	02:22:57
4	(PCI) bus transaction in opposite directions"	02:23:03
5	saying the PCI transaction is	02:23:04
6	communicated in serial form. That doesn't	02:23:08
7	constitute that a new standard is created calling	02:23:11
8	it a serial PCI bus, and I don't think there is	02:23:15
9	any attempt in here. This is something which was	02:23:19
10	invented in order to avoid all the complications	02:23:23
11	with big high pin count connectors limiting the	02:23:27
12	speed of communication for a very specific	02:23:31
13	purpose.	02:23:34
14	Q. As part of communicating the PCI	02:23:38
15	bus transaction in serial form, couldn't you	02:23:46
16	create or use virtual addressing as part of that	02:23:50
17	serial communication?	02:24:00
18	MR. DAVIS: Objection; form.	02:24:04
19	THE WITNESS: We have a bus here, which	02:24:07
20	is identified to address physical devices.	02:24:14
21	Communicating a virtual address on such a bus	02:24:21
22	would not allow the direct addressing of such	02:24:25
23	devices, therefore it wouldn't make any sense.	02:24:29
24	Basically all computers when communicating with	02:24:33
25	I/O devices have done their address translation	02:24:41

1	beforehand.	02:24:45
2	BY MR. BUROKER:	02:24:47
3	Q. So by that explanation, for this	02:24:47
4	claim to make sense, then no matter what device	02:24:52
5	receives this information, it has to be using	02:24:56
6	a PCI bus address that is understood and known by	02:25:03
7	the northbridge that sent it; is that right?	02:25:09
8	MR. DAVIS: Objection; form.	02:25:16
9	BY MR. BUROKER:	02:25:21
10	Q. Let me strike that and let me	02:25:21
11	start over.	02:25:22
12	So if I'm going to take a PCI bus	02:25:23
13	transaction and I'm going to serialize it, and on	02:25:25
14	the other side it's going to come back and be	02:25:29
15	recreated, any PCI device on the other end of	02:25:32
16	that serial transmission has to be using the same	02:25:34
17	addressing scheme as the transmitting side,	02:25:37
18	correct?	02:25:42
19	A. It's part of the overall address	02:25:43
20	map of the computer, correct. But	02:25:46
21	Q. So you couldn't have, in that	02:25:50
22	situation, a PCI device on one side of the serial	02:25:53
23	transmission and then one on the other one that	02:25:58
24	has the same address?	02:26:00
25	A. No.	02:26:02

1	Q. It wouldn't work?	02:26:04
2	A. Not a good thing.	02:26:04
3	Q. You would have a collision,	02:26:05
4	correct?	02:26:06
5	A. Correct. This is actually one of	02:26:07
6	the fundamental differences in the big new thing	02:26:09
7	which came about in the context of PCI because	02:26:14
8	that is one of the big issues we had with VME,	02:26:18
9	which is also part of the prior art being cited	02:26:21
10	here so it makes sense. In VME the address map	02:26:25
11	had to be defined before you switch on the	02:26:27
12	computer and you do this on a piece of paper and	02:26:29
13	then you had a little row of switches on all the	02:26:31
14	I/O devices where you defined this is your slave	02:26:35
15	address, and if by accident you enable two	02:26:39
16	devices on the same slave address you have a	02:26:41
17	non-working computer which even could end up in	02:26:44
18	hardware damage.	02:26:47
19	In PCI the system works differently.	02:26:47
20	When your computer wakes up all devices are	02:26:49
21	basically dead, disabled, do nothing. Then the	02:26:55
22	computer basically goes step by step through the	02:26:58
23	entire PCI tree, and this can be quite a few	02:27:00
24	devices, potential devices. It will address	02:27:03
25	every particular physical slot in the computer	02:27:07

1	connection device and this is why PCI has to have	02:27:11
2	geographic addressing which is part of the	02:27:16
3	configuration cycles. This is why I said	02:27:17
4	configuration is a little bit different in each	02:27:20
5	one. So the computer goes through every slot,	02:27:23
6	every potential location for an I/O device and	02:27:26
7	once it finds such a device, then it will check	02:27:30
8	what is the amount of local memory I/O space the	02:27:34
9	device has, collect all that information, then	02:27:38
LO	the BIOS creates an address map, based on some	02:27:41
11	algorithm which is not disclosed, and then it	02:27:46
L2	goes back and writes to every individual PCI	02:27:48
13	device, "This is now your base address on which	02:27:50
L 4	you respond if there is ever a PCI transaction."	02:27:53
15	And, of course, it's being made very sure that	02:27:56
16	under no circumstances windows overlap because	02:27:59
L7	then you have two devices answering and the	02:28:03
L8	result is garbage. That means, and this is why I	02:28:06
L 9	said earlier, without PCI configuration cycles	02:28:10
20	you have nothing, you have a dead system. And	02:28:12
21	that also means, taking into account now the	02:28:14
22	Horst reference, you have a million possible	02:28:17
23	nodes and each of those million nodes could have	02:28:20
24	several tens of possible PCI devices depending on	02:28:25
25	the complexity of the PCI tree, this what is	02:28:28

1	called device war would have to be done across	02:28:31
2	all these devices and it could only be done by	02:28:34
3	one because the address map is something which is	02:28:37
4	seen centric to one processor. So the entire PCI	02:28:42
5	architecture basically assumes there is one	02:28:45
6	processor at the top which defines the address	02:28:48
7	map. And even today in multiprocessor computers	02:28:50
8	it's exactly like that.	02:28:54
9	Q. The patent, both patents, give	02:29:12
10	examples of different ways of transmitting PCI	02:29:15
11	bus transaction in a serial form, we were looking	02:29:21
12	at 13, 14 and 15, Figures 13, 14, 15, right?	02:29:26
13	MR. DAVIS: Objection to form.	02:29:32
14	BY MR. BUROKER:	02:29:32
15	Q. For example.	02:29:32
16	A. Which patent?	02:29:34
17	Q. '814.	02:29:36
18	A. Okay, let me just pull this out.	02:29:38
19	Q. 13, 14 and 17, sorry.	02:29:43
20	A. You mean 13A and B?	02:29:51
21	Q. Actually, you know what, I think	02:29:53
22	it's the '873 Patent.	02:29:54
23	So, yeah, your paragraph 80 earlier, we	02:30:08
24	were looking at Figures 13 and 14 of the '873	02:30:12
25	Patent.	02:30:17

1	A. Yes.	02:30:17
2	Q. And then Figure 17 of the '814	02:30:17
3	Patent.	02:30:22
4	A. Yeah, these are just the	02:30:22
5	differential signals, right, the 17. Yeah.	02:30:29
6	Q. Well, 17 is showing what would be	02:30:33
7	used to generate the signals on the serial line,	02:30:38
8	right?	02:30:42
9	A. The clock and the four signals	02:30:43
10	conveying the actual	02:30:46
11	Q. Right, that would be a five-wire	02:30:49
12	system, and since there are five wires and	02:30:50
13	there's way more bits than that, that makes it	02:30:52
14	a serial transmission in your view; is that	02:30:56
15	correct?	02:30:58
16	A. Yeah, according to the definition	02:30:58
17	I set forth.	02:31:03
18	Q. Okay. And doesn't the	02:31:04
19	specification also say that the XP bus, which is	02:31:05
20	the serial bus in the patent, can use IEEE 1394?	02:31:11
21	MR. DAVIS: Objection; form.	02:31:20
22	THE WITNESS: Now, where does it say?	02:31:25
23	Where are we referring to and which patent?	02:31:27
24	BY MR. BUROKER:	02:31:31
25	Q. So '814, column 22, lines 7 to 8.	02:31:31

1	A. Column 2 you're saying?	02:32:05
2	Q. Column 22.	02:32:07
3	A. Sorry.	02:32:08
4	Q. Yes.	02:32:37
5	A. Yeah, I see that. I mean	02:32:37
6	basically what it says here is what we have here	02:32:40
7	is one way of communicating signals in a very	02:32:43
8	efficient and fast way, and this is not limited	02:32:46
9	to PCI itself, yeah.	02:32:49
10	Q. Right. So starting at column 22,	02:32:59
11	line 4, it says that:	02:33:01
12	"The XP Bus lines, PDO to PD3, PCN,	02:33:02
13	PDR0 to PDR3 and PCNR, and the video data and	02:33:15
14	clock lines, VPD and VPCK, are not limited to	02:33:20
15	being LVDS lines, as they may be other forms of	02:33:26
16	bit based lines. For example, in another	02:33:29
17	embodiment the XP Bus lines may be IEEE 1394	02:33:32
18	lines."	02:33:38
19	Right? That's saying that the bits	02:33:38
20	that are used to transmit the serial form of the	02:33:42
21	PCI bus can be IEEE 1394, FireWire line?	02:33:47
22	MR. DAVIS: Objection; form.	02:33:55
23	THE WITNESS: Do you have the 1394	02:33:58
24	standard right handy?	02:34:15
25	BY MR. BUROKER:	02:34:19

1	Q. I don't know that I do. You're	02:34:19
2	familiar with it obviously.	02:34:21
3	A. Sure.	02:34:21
4	Q. And what is it generally?	02:34:23
5	MR. DAVIS: Objection to form.	02:34:27
6	BY MR. BUROKER:	02:34:29
7	Q. I don't have a copy.	02:34:30
8	A. This evolved from the SCI	02:34:34
9	standards. Dave James, one of the main authors	02:34:38
10	of SCI, was also on the FireWire 1394 Committee I	02:34:41
11	believe when he still was working for Apple. The	02:34:46
12	reason why I wanted to have a quick look is to	02:34:48
13	refresh my mind about the exact physical	02:34:51
14	signalling definition in 1394.	02:34:53
15	The point here is obviously about the	02:35:02
16	definition, what is LVDS. And there is, on one	02:35:08
17	hand, the IEEE 1596.3 standard, which is, I	02:35:16
18	believe, the first incarnation of LVDS. In fact	02:35:25
19	that was just when I arrived in the U.S. as	02:35:31
20	a post-doc I was even part of that working group	02:35:33
21	and I saw the very first LVDS chips of national	02:35:35
22	semiconductors ever to exist, and they were	02:35:40
23	defined in the 1596.3 standard, a substandard of	02:35:42
24	SCI. Later, slightly different versions were	02:35:48
25	created, and I believe the patent says clearly	02:35:55

1	that in case of LVDS being cited they mean	02:35:58
2	generic low-voltage differential signals. So the	02:36:04
3	bottom line is, for example, 1596.3 says the	02:36:07
4	midpoint of that signal has to be at 1.2 volt and	02:36:12
5	the signal is, I believe, a one milliampere	02:36:15
6	signal, so if you want to move it to 1.5 volts it	02:36:19
7	wouldn't be LVDS any more according to 1596.3	02:36:22
8	but, from the context, from the logical meaning	02:36:26
9	what is low-voltage differential very	02:36:29
10	high-speed signals it would still be the same	02:36:36
11	thing.	02:36:38
12	So what they try to say here is, in my	02:36:38
13	understanding, if a slight variation of the	02:36:43
14	physical signalling from the original standard,	02:36:45
15	it would still work the same way, it would still	02:36:51
16	make sense.	02:36:56
17	I'm trying to find now the definition in	02:36:57
18	this patent, how they interpret LVDS, but I'm	02:36:59
19	very sure there is a definition and it says that.	02:37:02
20	Q. Well, in paragraph 81 of your '814	02:37:08
21	declaration, it says:	02:37:13
22	"The '873 patent discusses serial lines	02:37:21
23	and serial packet protocols and uses LVDS IEEE	02:37:24
24	1394 (FireWire) and Universal Serial Bus as	02:37:29
25	examples."	02:37:33

1	And then you cite to the '814 Patent	02:37:34
2	column 22, 26 to 30. I don't know if that's	02:37:37
3	helpful.	02:37:44
4	And then it says:	02:37:45
5	" LVDS encodes serial bits as	02:37:48
6	voltage differences onto opposed lines such as in	02:37:51
7	Figure 15 of the '873 patent."	02:37:54
8	A. You got me lost, I wasn't fast	02:37:56
9	enough for you. Which page are we now?	02:37:59
10	Q. Paragraph 81, page 49.	02:38:01
11	A. '814, 22, 26 to 30. Yeah, I mean	02:38:59
12	here they also say they are examples but they	02:39:12
13	don't limit themselves to any particular special	02:39:15
14	incarnation.	02:39:20
15	Q. Does IEEE 1394 support 32-bit PCI	02:39:22
16	flat addressing?	02:39:30
17	A. Now, I would really like to look	02:39:34
18	at that specification. Off the top of my head	02:39:35
19	this is a different thing and I would expect not,	02:39:37
20	but I would rather look at the specification.	02:39:42
21	Q. I don't have it, I apologize.	02:39:46
22	A. Do we have it?	02:39:47
23	Q. I don't. And that's fair. As you	02:39:48
24	sit here today, you don't know whether or not	02:39:59
25	IEEE 1394 supports the 32-bit PCI flat addressing	02:40:01

1	space or not. It may or may not, is that fair?	02:40:07
2	A. Yeah.	02:40:09
3	Q. Okay. Do you know whether IEEE	02:40:11
4	1394 can contain PCI standard addresses or	02:40:21
5	standard bus commands?	02:40:26
6	MR. DAVIS: Objection; form.	02:40:28
7	THE WITNESS: And I would again like to	02:40:32
8	refer to the specification. If I had a computer	02:40:33
9	I could pull it from the net real quick.	02:40:36
10	This is an SCI-like network, so	02:40:40
11	consequently, given the arguments I set forth	02:40:48
12	here, most likely they are the same.	02:40:52
13	BY MR. BUROKER:	02:40:57
14	Q. So you say "set forth here", your	02:40:57
15	hand is on your declaration, meaning the	02:40:59
16	arguments you made about SCI in your declaration	02:41:01
17	about why it doesn't meet the claims you would	02:41:03
18	think that IEEE 1394 doesn't meet the claims?	02:41:07
19	A. Yeah, but I mean I'm under oath	02:41:11
20	here, I really don't want to do too much	02:41:16
21	speculation and although I am obviously quite	02:41:18
22	familiar with FireWire, I would rather stick to	02:41:26
23	the documents and if we can't have them it's	02:41:30
24	going to be a bit too much vague, I think.	02:41:31
25	MR. BUROKER: Okay. I may come back to	02:41:36

1	it, I can always print at some later time or for	02:41:38
2	tomorrow, so we'll see.	02:41:43
3	I need to take a break right now	02:41:45
4	though. Can we go off the record?	02:41:47
5	(Brief recess taken 2:41 p.m 2:51 p.m.)	02:41:48
6	BY MR. BUROKER:	02:51:53
7	Q. So, paragraph 82 of your	02:51:55
8	declaration it may be even on the same page,	02:51:57
9	great you talk about one of the advantages of	02:52:01
10	the patented system is that, in the second	02:52:12
11	sentence you say:	02:52:18
12	" no new drivers are needed to	02:52:19
13	ensure the peripherals work on the system."	02:52:22
14	Do you see that?	02:52:24
15	A. Absolutely, yes.	02:52:25
16	Q. Okay. So, as you read the '814,	02:52:26
17	and '873 Patents, did the inventor create any	02:52:34
18	additional drivers or not?	02:52:43
19	A. I believe they even make the point	02:52:44
20	this is not necessary and this is a big advantage	02:52:46
21	because otherwise the ACM couldn't use any	02:52:49
22	generic device being connected to the console	02:52:56
23	where it's plugged in. Now let me see if I can	02:53:00
24	find this quickly. Probably you know this even	02:53:02
25	better than me, but it's definitely in I	02:53:04

1	believe it's in both of them.	02:53:08
2	Q. Well you cite in your declaration	02:53:10
3	to the '873 Patent at column 4, lines 50 to 58.	02:53:12
4	A. So I should just read my own	02:53:20
5	declaration and use the references right there.	02:53:22
6	Yeah, I think the relevant sentence	02:54:18
7	would be:	02:54:20
8	"The invention also can be implemented	02:54:21
9	without changes in operating system and	02:54:23
10	application software."	02:54:26
11	Now, that clearly means device drivers	02:54:28
12	because they're part of the operating system and	02:54:31
13	being loaded on demand depending on in fact PCI	02:54:34
14	configuration cycle.	02:54:40
15	Q. Looking now at the claims we've	02:54:44
16	been looking at, take for example claim 24 of the	02:54:48
17	'814, is there anything in the claim that says	02:54:52
18	you can't have new drivers or that, you know, the	02:54:58
19	system has to be interoperable with existing	02:55:02
20	software?	02:55:06
21	MR. DAVIS: Objection; form.	02:55:11
22	THE WITNESS: I just read it again to	02:55:13
23	be really sure. It doesn't say explicitly, but	02:55:45
24	since we have the transmission of encoded PCI bus	02:55:52
25	transactions, that means the PCI infrastructure	02:55:59

1	is maintained and that would have a direct	02:56:06
2	consequence. But it's not an explicitly stated	02:56:10
3	requirement of claim 24.	02:56:18
4	BY MR. BUROKER:	02:56:18
5	Q. Okay. And then your declaration	02:56:20
6	also makes mention about the fact that there is	02:56:22
7	no need for any new hardware; is that correct?	02:56:27
8	A. In what context?	02:56:37
9	Q. Well, in paragraph 97 and 98, one	02:56:43
10	of the points you make about the difference	02:56:58
11	between the patented invention and the TNet	02:57:01
12	system is that the TNet required new hardware to	02:57:04
13	operate; is that correct?	02:57:07
14	A. Yeah, correct.	02:57:09
15	Q. Is there anything in claim 24 of	02:57:10
16	the '814 Patent that excludes the addition of new	02:57:13
17	hardware?	02:57:18
18	A. There is no statement about that	02:57:27
19	in this claim.	02:57:30
20	Q. And what about 31 of the '814	02:57:32
21	Patent?	02:57:34
22	A. Same here, no explicit language,	02:57:58
23	although since we are conveying complete PCI bus	02:57:59
24	transactions it would be implicitly the case.	02:58:05
25	Why build it? There's no need to build	02:58:08

1	additional hardware to generate the PCI	02:58:13
2	transactions, because it's already here, this is	02:58:15
3	the point I'm trying to make, all right? In this	02:58:17
4	case PCI bus transactions are communicated over	02:58:20
5	these kind of channels, it is spelt out in	02:58:23
6	slightly different forms, but it's always the	02:58:27
7	same basic principle, enabling the receiving	02:58:29
8	device to produce that particular piece of	02:58:36
9	transaction completely transparently to hardware	02:58:40
10	and software. Therefore there is no need to do	02:58:45
11	anything else. In case	02:58:48
12	Q. Well if the I'm sorry.	02:58:49
13	A. In case of both SCI and TNet,	02:58:51
14	there is an entirely radically different topology	02:58:54
15	in architecture and for it to interface to PCI	02:59:00
16	one has to have a particular device creating such	02:59:04
17	PCI transactions based on some macro commands	02:59:07
18	being sent over that network.	02:59:09
19	Q. But even the invention	02:59:12
20	contemplates some additional hardware; there's	02:59:16
21	the hardware that serializes the PCI bus	02:59:18
22	transaction. That's a new piece of hardware,	02:59:21
23	right?	02:59:23
24	A. That is correct.	02:59:23
25	Q. So what did you mean by saying	02:59:24

1	that unlike the invention TNet requires new	02:59:25
2	hardware?	02:59:30
3	MR. DAVIS: Objection; form.	02:59:32
4	THE WITNESS: Now, let me just check,	02:59:38
5	are we discussing here in context of TNet or in	02:59:46
6	context of SCI? I think this is TNet, right?	02:59:50
7	BY MR. BUROKER:	02:59:56
8	Q. Correct.	02:59:56
9	A. Right, so these interfaces here	02:59:57
10	have to have quite a bit of functionality, there	03:00:02
11	is no direct obvious one-to-one A-B-C-D kind of	03:00:06
12	path as to how they are to be built. They have	03:00:13
13	to be able to execute all the specified PCI	03:00:16
14	transactions on the remote PCI bus, but these	03:00:21
15	transactions do not exist inside the TNet system	03:00:24
16	area network. There is on top of that an address	03:00:28
17	translation which needs to be done in the peer	03:00:31
18	system, let alone it being initialized and	03:00:35
19	everything. For it to be performing there is	03:00:39
20	typically a very large complexity of additional	03:00:43
21	functionality needed for this to make any sense.	03:00:47
22	So this is a highly complex ASIC.	03:00:51
23	What is outlined in this patent is	03:00:57
24	complex also, but we are basically serializing	03:00:59
25	the particular ongoing PCI transaction which is	03:01:03

1	being then made parallel on the far end again.	03:01:05
2	This is a different thing, there is no address	03:01:09
3	translation for instance involved and all the	03:01:11
4	other things. We can go into details here, if	03:01:12
5	you want, to make this more clear.	03:01:15
6	Q. But my strike that.	03:01:23
7	My question was more, on paragraph 97,	03:01:25
8	for example, it talks about avoiding the	03:01:27
9	requirement imposed by TNet of designing new bus	03:01:34
10	interface devices and new device drivers, but do	03:01:40
11	you agree that to implement the '814 patent you	03:01:43
12	still have to create a new hardware system to	03:01:50
13	serialize the PCI bus transaction on one end and	03:01:53
14	then interpret it on the other to output the PCI	03:01:56
15	bus transaction on the receiving end, right?	03:02:01
16	MR. DAVIS: Objection; form.	03:02:03
17	THE WITNESS: The '814 Patent outlines	03:02:06
18	how to build the serializer, this is correct.	03:02:14
19	BY MR. BUROKER:	03:02:14
20	Q. So there is some new piece of	03:02:17
21	hardware, software, whatever it is, the	03:02:18
22	serializer is something new?	03:02:20
23	A. Not software, hardware.	03:02:21
24	Q. So in the '814 Patent the patent	03:02:51
25	talks about the host interface controller and	03:02:57

1	then the peripheral interface controller, the HIC	03:03:00
2	and the PIC, are you familiar with those?	03:03:04
3	A. Uh-huh, let me just pull it.	03:03:08
4	Okay, here we are.	03:03:10
5	Q. So those are not off-the-shelf	03:03:15
6	components, correct?	03:03:18
7	A. Now, let me just see where exactly	03:03:21
8	are we talking to?	03:03:24
9	Q. Well they talk about them quite	03:03:27
10	a bit in the patent, so the HIC and the PIC.	03:03:28
11	A. Just to start at some particular	03:03:35
12	reference to be on the same page.	03:03:42
13	Q. Which patent are you looking at?	03:03:44
14	A. '814. Didn't you say '814?	03:03:46
15	Q. That's fine. So they're shown in	03:03:49
16	Figure 7 is one place. And they're in 21 and 22,	03:03:52
17	they're in a number of places.	03:04:16
18	A. My '814 patent doesn't have	03:04:18
19	a Figure 7. 3, 4, 5, 5A, 6, 8.	03:04:20
20	Q. Oh you know what, I was looking at	03:04:26
21	the '873, I apologize. Let me look at the '814.	03:04:28
22	So if you look at Figure 15, for	03:04:55
23	example, the top section is the host interface	03:04:58
24	controller and the bottom section is the	03:05:00
25	peripheral interface controller.	03:05:03

1	A. Okay.	03:05:12
2	Q. So the question is: those are not	03:05:13
3	described as being off-the-shelf components in	03:05:15
4	this patent, are they?	03:05:18
5	A. No. In particular, I mean, the XP	03:05:22
6	bus is part of the patent, so this is something	03:05:25
7	novel.	03:05:28
8	Now, I can't tell whether or not Acqis	03:05:30
9	decided to make those commercial products and	03:05:34
10	sell them off the shelf, so from that point of	03:05:36
11	view I can't answer the question. But it's	03:05:38
12	certainly not a generic something.	03:05:41
13	Q. Right. So, in other words to make	03:05:43
14	at least the embodiments disclosed in this figure	03:05:45
15	work they had to create a host interface	03:05:50
16	controller, the XP bus and a peripheral interface	03:05:54
17	controller, so three pieces of hardware, right?	03:05:58
18	A. There is quite a bit of similarity	03:06:02
19	between these tools, so it's probably two	03:06:04
20	versions of one common reference, right? I mean	03:06:06
21	the bus controller, which is a bi-directional	03:06:08
22	bus, will be mostly the same except for the clock	03:06:12
23	generation, which is detailed in here, the PCI	03:06:15
24	interface is the same anyway. So from that point	03:06:21
25	of view they are rather similar but, yes, they	03:06:23

1	are different devices which are needed for this	03:06:26
2	communication to happen.	03:06:28
3	Q. So like TNet, where you had to	03:06:34
4	create additional hardware, this invention also	03:06:37
5	contemplates creating additional hardware in	03:06:40
6	order to send the PCI bus transaction in serial	03:06:43
7	form, right?	03:06:47
8	A. This invention transmits PCI	03:06:52
9	transactions in serial form, TNet does not.	03:06:57
10	Q. Right, but this invention, in	03:06:59
11	order to do so, had to create new hardware to	03:07:01
12	make that possible?	03:07:03
13	A. I agree with that.	03:07:05
14	Q. Right, you've got the Horst/TNet	03:07:13
15	reference in front of you?	03:07:17
16	A. Horst/TNet, here we are.	03:07:27
17	Q. So one of the things you say in	03:07:55
18	your declaration, and in particular and I'll	03:07:57
19	give you the paragraph number is that the TNet	03:07:59
20	bus interface in the console generates a PCI bus	03:08:03
21	transaction; is that correct.	03:08:11
22	A. Where is that?	03:08:13
23	Q. Paragraph 133.	03:08:15
24	A. And we are still	03:08:16
25	Q. Oh '814 declaration,	03:08:17

1	paragraph 133.	03:08:20
2	A. Right:	03:08:37
3	"The TNet bus interface then uses its	03:08:37
4	knowledge of the PCI bus and the PCI bus protocol	03:08:40
5	to generate a PCI bus transaction on the PCI	03:08:44
6	bus."	03:08:47
7	Q. Maybe it's easier if we just walk	03:08:49
8	through your understanding of how something would	03:08:52
9	work.	03:08:57
10	So looking at Figure 2 of the Horst	03:09:01
11	reference. Okay, so what is shown there is CPU	03:09:07
12	memory boxes up top. Those are what EMC contends	03:09:14
13	to be the modules, correct?	03:09:24
14	MR. DAVIS: Objection; form.	03:09:27
15	BY MR. BUROKER:	03:09:30
16	Q. In the claim there is an ACM	03:09:30
17	module, an ACM?	03:09:33
18	A. Yeah, I very well remember that.	03:09:36
19	We're talking the '814 here, right?	03:09:38
20	Q. Uh-huh.	03:09:42
21	A. So let me just pull this up	03:09:43
22	because I believe the definition of the ACM is in	03:09:46
23	the claim and it required a bit more than just	03:09:48
24	CPU and memory. And, I mean, this is a very,	03:09:50
25	very high-level diagram, so one has to be always	03:09:56

1	careful with these high abstraction levels. One	03:09:59
2	can interpret a lot into them which may not	03:10:02
3	really be there at the end.	03:10:06
4	So let me just check.	03:10:07
5	" the console comprising a first low	03:10:15
6	voltage differential signal channel	03:10:18
7	comprising two unidirectional serial channels	03:10:20
8	that transmit encoded data of (PCI) bus	03:10:22
9	transaction in opposite directions; said ACM	03:10:25
10	comprising a microprocessor unit a mass	03:10:29
11	memory storage device"	03:10:31
12	Which is not here on top of Figure 2:	03:10:32
13	" a north bridge to communicate	03:10:38
14	address and data bits of PCI"	03:10:39
15	Neither a northbridge is shown here nor	03:10:41
16	PCI is shown here. In fact it is shown that	03:10:45
17	these two links go to two apparently different,	03:10:47
18	possibly redundant, TNet sub-nets and that	03:10:54
19	clearly rules out PCI to be there.	03:10:59
20	" a main memory coupled to said	03:11:02
21	processor unit through said north bridge"	03:11:04
22	Now here's the limitation that the main	03:11:07
23	memory has to be coupled to the CPU through the	03:11:08
24	northbridge, there's no northbridge shown but,	03:11:11
25	again, at this abstraction layer it could have	03:11:12

1	been just omitted. It wouldn't be something	03:11:15
2	extremely uncommon to use a northbridge. A	03:11:19
3	second LVDS channel, again to communicate PCI bus	03:11:23
4	transaction. So, taking claim 24 as the first	03:11:29
5	big independent claim of that patent, I would say	03:11:34
6	this cannot be an ACM.	03:11:36
7	Q. Looking at Figure 7 then, which is	03:11:38
8	a little bit of a more blown up or detailed view	03:11:43
9	of the various components.	03:11:47
10	A. Okay.	03:11:49
11	Q. Let's just suppose that that RISC	03:11:54
12	CPU wants to talk to a PCI device that's	03:11:58
13	connected to the TNet links and the PCI device	03:12:13
14	would be something hanging off the bottom of	03:12:17
15	what's shown in Figure 8.	03:12:19
16	MR. DAVIS: Objection; form.	03:12:24
17	THE WITNESS: Now careful; Figure 8 is	03:12:34
18	VME.	03:12:37
19	BY MR. BUROKER:	03:12:40
20	Q. No, Figure 8 says it can be	03:12:41
21	connected to a 32-bit bus which can be VME,	03:12:43
22	Motorola 68040 or PC it says PCL but it's	03:12:51
23	referring to PCI.	03:12:54
24	MR. DAVIS: Objection to form.	03:12:55
25	THE WITNESS: You mean this is a typo?	03:12:56

1	BY MR. BUROKER:	03:12:58
2	Q. Yes.	03:12:58
3	A. A typo?	03:12:58
4	Q. You can go to the text, if you	03:12:59
5	like, just to the left of that. The text says:	03:13:00
6	"Figure 8 shows a block diagram of the	03:13:03
7	TNet bus interface (TBI) ASIC. The TBI	03:13:05
8	translates transfers on the standard bus into	03:13:12
9	TNet read or write transactions that travel	03:13:14
10	through TNet links to main memory.	03:13:17
11	"Different versions of the bus	03:13:18
12	interface logic support industry standard buses	03:13:20
13	such as VME and the peripheral component	03:13:24
14	interconnect (PCI), or microprocessor buses such	03:13:27
15	as that of the Motorola 68040 chip."	03:13:32
16	Do you see that?	03:13:36
17	A. Okay.	03:13:38
18	Q. So that "PCL" is a typo. It	03:13:38
19	should be "PCI".	03:13:40
20	MR. DAVIS: Objection; form.	03:13:40
21	BY MR. BUROKER:	03:13:40
22	Q. Do you agree?	03:13:41
23	MR. DAVIS: Objection; form.	03:13:42
24	THE WITNESS: Given that the text	03:13:49
25	clearly describes that, then I would take this as	03:13:52

1	a high-level diagram which says there are	03:13:57
2	different versions of this obviously, which	03:14:01
3	probably have different bus interfaces sitting	03:14:03
4	next to each other on that ASIC in order to	03:14:07
5	generate the particular type of bus transaction	03:14:13
6	required.	03:14:16
7	BY MR. BUROKER:	03:14:17
8	Q. Right. And looking back at	03:14:17
9	Figure 2, it shows an example of one of those	03:14:19
10	interfaces you're talking about, it shows a box	03:14:24
11	that says "PCI interface", do you see that?	03:14:27
12	A. Yes, at the right bottom.	03:14:30
13	Q. So looking at the Figure 8 in	03:14:35
14	combination with Figure 2, what you're saying is	03:14:38
15	there would be a PCI interface box that would be	03:14:40
16	attached to the long line in Figure 8. Is that	03:14:42
17	correct?	03:14:48
18	MR. DAVIS: Objection; form.	03:14:49
19	THE WITNESS: There would be a PCI	03:14:57
20	interface connected to this bus line, the long	03:14:59
21	line as you call it, drawn in Figure 8, yeah.	03:15:03
22	Assuming that "PCL" is a typo, correct.	03:15:07
23	BY MR. BUROKER:	03:15:15
24	Q. And then connected to that PCI bus	03:15:15
25	interface would be potentially one or more PCI	03:15:19

1	devices?	03:15:22
2	A. Correct.	03:15:22
3	Q. So both Figure 7 and Figure 8	03:15:30
4	refer to or point to this thing that says TNet	03:15:34
5	links?	03:15:38
6	A. Correct.	03:15:39
7	Q. So the idea is that what's shown	03:15:40
8	in Figure 7 would connect to the TNet links to	03:15:42
9	what is shown at Figure 8. Is that the right way	03:15:46
10	to read this?	03:15:49
11	MR. DAVIS: Objection; form.	03:15:50
12	THE WITNESS: I mean TNet is a defined	03:15:52
13	protocol here and now I purposefully avoid the	03:15:56
14	word "standard" because, you know, it's	03:16:00
15	proprietary I assume. But it's defined, at least	03:16:04
16	within the context of this document, and so TNet	03:16:08
17	link in Figure 8 would have to be the same thing	03:16:12
18	as TNet link in Figure 7 and they would have to	03:16:16
19	be interoperable for this to make any sense.	03:16:20
20	BY MR. BUROKER:	03:16:20
21	Q. And then what's shown in Figure 2,	03:16:23
22	those long rectangles, are described as TNet	03:16:26
23	links in the document.	03:16:29
24	THE WITNESS: Careful, this is	03:16:31
25	MR. BUROKER: Is that right?	03:16:33

1	MR. DAVIS: Objection; form.	03:16:34
2	THE WITNESS: this is the TNet	03:16:36
3	system area network, where the TNet links are	03:16:39
4	only a small fraction of. The link is basically	03:16:42
5	just the way to connect to the system, and I mean	03:16:46
6	the network system here.	03:16:52
7	Again, also here, we are talking very	03:16:56
8	fast links which are point-to-point. So in order	03:16:59
9	to be able to have a large number of particular	03:17:03
10	devices talking to each other, typically with	03:17:06
11	lots of processors, there has to be some kind of	03:17:08
12	a network, with switches, routers and everything.	03:17:11
13	Figure 9 gives a rough outline of this. And the	03:17:15
14	fact that Figure 2 shows two different networks	03:17:18
15	here, X and Y, indicates that there is	03:17:24
16	a redundancy in the network, allowing packets to	03:17:33
17	travel different paths from source destination,	03:17:36
18	which is something people like to do in order to	03:17:40
19	have flexibility and in order to avoid	03:17:45
20	congestion, taking the B path if A is overloaded,	03:17:52
21	which has lots of highly complex ramifications.	03:17:56
22	So in here is a rather complex networking in	03:17:58
23	between. You see in Figure 9 six routers being	03:18:03
24	drawn. Whatever number there is depends on the	03:18:06
25	architecture of the switching technology being	03:18:12

1	developed for TNet, but there is absolutely	03:18:14
2	nothing disclosed, if I remember correctly,	03:18:17
3	inside this document as to how these switches	03:18:21
4	would really work in detail, except for this very	03:18:23
5	high-level diagram in Figure 6. Which is	03:18:29
6	a diagram which is basically valid for every kind	03:18:34
7	of switch in any kind of networking standard.	03:18:36
8	BY MR. BUROKER:	03:18:36
9	Q. Okay. So one configuration is	03:18:43
10	possible to have a single to have the elements	03:18:51
11	of Figure 7 connected directly over TNet links to	03:18:57
12	what's shown in Figure 8 and then have Figure 8	03:19:05
13	connected to a PCI bus interface which would be	03:19:10
14	connected to a PCI device?	03:19:14
15	MR. DAVIS: Objection	03:19:18
16	BY MR. BUROKER:	03:19:19
17	Q. Is that right?	03:19:19
18	MR. DAVIS: Objection; form.	03:19:20
19	THE WITNESS: Honestly I can't tell.	03:19:22
20	The reason is it depends really on a lot of	03:19:25
21	details as how this network is being built.	03:19:33
22	There are networks which do not allow direct	03:19:38
23	node-to-node connection. Basically what you're	03:19:42
24	saying do away without the switching and the	03:19:44
25	infrastructure and do a point-to-point	03:19:47

1	connection, I understand that. Some networks	03:19:50
2	allow doing that, some don't. Whether TNet	03:19:53
3	supports this functionality is not disclosed in	03:19:56
4	this document.	03:19:58
5	BY MR. BUROKER:	03:19:58
6	Q. So the fact that there's the word	03:20:01
7	"TNet link" in Figure 8 and the word "TNet link"	03:20:03
8	in Figure 7, you can't tell, is what you're	03:20:07
9	saying, whether or not that means that they can	03:20:09
10	be directly coupled together without more	03:20:11
11	information?	03:20:13
12	MR. DAVIS: Objection; form.	03:20:13
13	THE WITNESS: "TNet link" only means	03:20:16
14	the connection for the network, very	03:20:19
15	oversimplifying the network cable. But I mean it	03:20:25
16	is more, right, the entire definition of the	03:20:26
17	standard, protocols, and so forth. Whether or	03:20:28
18	not you can directly connect them it doesn't	03:20:32
19	implicitly say. So at the time this was	03:20:37
20	invented, for example, it was not possible to	03:20:41
21	connect two computers with a twisted pair	03:20:45
22	Ethernet cable.	03:20:53
23	(The court reporter sought clarification.)	03:20:53
24	THE WITNESS: Sorry, a twisted pair	03:20:53
25	Ethernet cable. You had to have what is called	03:20:53

1	a crossover cable, where a couple of wires were	03:20:55
2	changed. Now since this is not necessary these	03:21:00
3	days anymore because the network devices in	03:21:03
4	computers basically test which kind of cable is	03:21:07
5	being plugged in and then they automatically	03:21:12
6	electronically change internally.	03:21:14
7	BY MR. BUROKER:	03:21:14
8	Q. But would a person of skill in the	03:21:19
9	art in '96, as you've defined it, be able to look	03:21:22
10	at this document and determine how to connect	03:21:26
11	what's shown in Figure 7 directly to Figure 8?	03:21:29
12	MR. DAVIS: Objection to form.	03:21:34
13	THE WITNESS: From the level of	03:21:40
14	disclosure in this document, I, as expert, cannot	03:21:45
15	tell whether this is possible, so a person of	03:21:47
16	ordinary skill in the art I doubt would be able	03:21:49
17	to tell. You know one could try and see whether	03:21:51
18	it worked.	03:21:53
19	BY MR. BUROKER:	03:21:56
20	Q. Okay, but you agree that Figure 9	03:21:57
21	shows an architecture in which the processor	03:22:02
22	interface, which is the one shown in Figure 7, is	03:22:06
23	connected via several routers to a bus interface	03:22:12
24	which is what's shown in Figure 8?	03:22:18
25	A. That's correct.	03:22:21

1	Q. And the bus interface in Figure 9	03:22:23
2	could be a PCI bus interface, because that's one	03:22:26
3	of the examples that the text tells us can be	03:22:32
4	part of Figure 8, correct?	03:22:36
5	A. Correct, although in this case,	03:22:38
6	SCSI is used as an example, yeah, there I agree.	03:22:42
7	Q. So if you were going to have a PCI	03:22:44
8	bus interface in Figure 9 then you would connect	03:22:49
9	it to one or more PCI devices and not one or more	03:22:52
10	SCSI devices, right?	03:23:01
11	A. Yeah.	03:23:01
12	MR. BUROKER: SCSI is S-C-S-I, all	03:23:02
13	caps.	03:23:02
14	THE COURT REPORTER: Thank you.	03:23:02
15	BY MR. BUROKER	03:23:02
16	Q. It's shorthand for what does	03:23:04
17	"SCSI" stand for?	03:23:06
18	A. I believe "small computer system	03:23:08
19	interface", but I wouldn't bet on it. This is	03:23:10
20	a mass storage standard.	03:23:14
21	Q. Everybody just calls them SCSI.	03:23:21
22	A. Yeah. It's a byte-wide kind of	03:23:24
23	bus.	03:23:30
24	Q. So with that in mind, if you have	03:23:31
25	the Figure 7 RISC CPU, you place that in as	03:23:33

1	connected to the processor in Figure 9. You have	03:23:44
2	in mind what I'm talking about?	03:23:46
3	A. Yes, you're trying to replace the	03:23:48
4	top three top two boxes.	03:23:49
5	Q. Uh-huh.	03:23:52
6	A. One being CPU memory and the other	03:23:53
7	being processor interface with	03:23:55
8	Q. What's in Figure 7.	03:23:57
9	A what's in Figure 7, yeah.	03:23:58
10	Q. So if you had that, and that RISC	03:24:00
11	CPU wanted to communicate to a PCI device in the	03:24:04
12	example where the bus interface is a PCI bus	03:24:09
13	interface and then, instead of SCSIs, you've got	03:24:12
14	a PCI device connection, correct?	03:24:15
15	A. Yeah.	03:24:17
16	Q. And in that situation then the bus	03:24:20
17	interface would be what's shown in Figure 8 as	03:24:28
18	the TNet bus interface and then the line would be	03:24:31
19	a PCI line and there would be a PCI device	03:24:36
20	connected to that? So you got that scenario in	03:24:42
21	mind?	03:24:45
22	A. (The witness nodded.)	03:24:45
23	Q. Okay. If this RISC CPU wanted to	03:24:46
24	do a write transaction to that PCI device	03:24:58
25	A. Uh-huh.	03:25:04

1	Q what information would it send	03:25:06
2	to the processor interface?	03:25:09
3	MR. DAVIS: Objection; form.	03:25:13
4	THE WITNESS: With "processor	03:25:18
5	interface" you mean the system bus in Figure 7,	03:25:20
6	for instance, right?	03:25:23
7	BY MR. BUROKER:	03:25:24
8	Q. It would be the well, yeah, it	03:25:24
9	would be the system bus interface that is part of	03:25:30
10	the TNet processor interface in Figure 7, right.	03:25:33
11	That whole grey area is the TNet processor	03:25:39
12	interface according to this diagram.	03:25:44
13	A. Yeah, yeah, I understand that very	03:25:47
14	well.	03:25:48
15	Q. Right.	03:25:49
16	A. But here starts the problem.	03:25:50
17	First of all, in order for the processor to talk	03:25:53
18	to any particular device, the processor has to	03:25:57
19	know the physical address of that particular	03:26:02
20	device as seen from its own local address space,	03:26:06
21	right? The processor lives in its own address	03:26:15
22	space, which means potentially all one million	03:26:19
23	processors inside TNet live in their own	03:26:22
24	individual one million possibly different address	03:26:25
25	spaces because they don't all have to be the	03:26:26

1	same. So the fundamental question is what is the	03:26:29
2	address of the particular PCI device connected to	03:26:33
3	this TNet system, possibly having lots of such	03:26:39
4	devices, as seen from the processor in this	03:26:44
5	particular system at its particular system bus.	03:26:48
6	Because the processor doesn't say, "I want to	03:26:52
7	talk to the TNet interface", the processor says,	03:26:55
8	"Here is an address" and then the rest of the	03:26:59
9	system has to handle that. In order to get	03:27:01
10	there, the PCI device first of all has to be	03:27:05
11	initialized, right? When you switch it on it's	03:27:10
12	dead, it says, "Leave me alone, I do not nothing	03:27:13
13	but respond to PCI configuration cycles." Now,	03:27:15
14	now this device has no way of directing any kind	03:27:19
15	of PCI configuration cycles on the remote device	03:27:22
16	of TNet.	03:27:25
17	Q. When you say "this device" you're	03:27:26
18	pointing at what?	03:27:28
19	A. I'm pointing to the RISC CPU.	03:27:28
20	Q. Go ahead?	03:27:28
21	A. So for this to be initialized,	03:27:33
22	which would be the first step prior to anything	03:27:36
23	that could possibly happen, one has to understand	03:27:38
24	how the people who developed that TNet-to-PCI	03:27:40
25	interface conceived how this should happen.	03:27:45

1	There is no clear path to this solution, there	03:27:47
2	are many possible solutions. One example would	03:27:52
3	be, since you asked me as an expert in the field,	03:27:57
4	is that this interface has a variety of	03:28:01
5	particular configuration areas, and don't forget	03:28:06
6	the RISC CPU in Figure 7 of the TNet reference	03:28:12
7	has no way of generating a configuration cycle	03:28:16
8	for that matter; it just does its own processor	03:28:20
9	cycles, a completely different thing. Other bus,	03:28:24
10	other bus states, other everything. So it would	03:28:28
11	first of all know how to talk to the PCI	03:28:31
12	interface on the TNet site. That would require	03:28:35
13	the TNet system to be initialized, all the	03:28:38
14	address translation tables to be initialized, all	03:28:43
15	the nodes IDs of all nodes connected to TNet to	03:28:45
16	be given a unique address, nothing it disclosed	03:28:49
17	in here how this is possibly being done, and this	03:28:51
18	is a highly complex problem, again because at	03:28:55
19	this point in time there can only be one agent	03:28:59
20	reasonably distributing those addresses,	03:29:02
21	otherwise you have an address collision, very	03:29:05
22	simple, which triggers the question who is the	03:29:07
23	chosen one? There is a long paragraph about this	03:29:10
24	complexity in the SCI standard if you want to	03:29:13
25	read it.	03:29:16

_	50 you have to initialize first the	03:29:16
2	entire TNet system, set up all address	03:29:19
3	translation tables, have to define address	03:29:21
4	windows to reach the particular TNet nodes in	03:29:23
5	this particular case because the PCI-to-TNet	03:29:30
6	nodes have to be set up right. That would enable	03:29:36
7	then the RISC CPU to communicate via read and	03:29:39
8	write commands to the PCI-TNet interface, which	03:29:44
9	would show up somewhere in the address space, in	03:29:47
LO	the physical address space of the RISC CPU in	03:29:50
L1	Figure 7. This is the first step.	03:29:54
L2	Then the RISC CPU in Figure 7 would have	03:29:56
L3	to communicate with the PCI-TNet interface	03:30:00
L 4	saying, "Actually I would like to do a PCI	03:30:03
L 5	cycle". And to start with it would have to be	03:30:06
L 6	a PCI configuration cycle and it would have to go	03:30:08
L7	through all possible slots available. And for	03:30:11
L 8	every cycle it would get a response. Again there	03:30:18
L 9	is many different ways. One way is, for example,	03:30:21
20	that the particular PCI command is uploaded into	03:30:23
21	the interface to some defined subaddress space	03:30:27
22	and then by writing to some key address the	03:30:31
23	interface executes now this PCI transaction and	03:30:34
24	leaves the result in another register inside this	03:30:37
25	ASIC, and then the processor comes back again,	03:30:40

1	reading this register saying, "What was the	03:30:43
2	result of my command?" Right? So basically it	03:30:45
3	would prepare the transaction that could be	03:30:49
4	multiple write transactions to configure the	03:30:51
5	device, and could also envision also solutions,	03:30:56
6	but this is one example.	03:30:58
7	Now we have found there is a PCI device	03:31:00
8	on that bus. The next step is run configuration	03:31:03
9	cycles against the device to find out how much	03:31:05
10	memory the device has in order to now map this in	03:31:07
11	the context of the complete TNet address space	03:31:12
12	and we have to keep in mind that the virtual	03:31:17
13	addresses inside TNet have to be encoded on the	03:31:20
14	have to be generated on the host site, so that	03:31:24
15	the target device is properly received.	03:31:28
16	Once all of that has been done then	03:31:31
17	there would be possibly a region in the address	03:31:35
18	space of the RISC CPU, which would enable it to	03:31:40
19	perform a write transaction which would then	03:31:45
20	subsequently be captured by the TNet processor	03:31:50
21	interface as shown in Figure 7. Now the CPU	03:31:57
22	obviously knows the right addresses, it would	03:32:00
23	then be translated by this TNet processor	03:32:02
24	interface, the addresses would be converted into	03:32:06
25	TNet addresses, this is a table lookup	03:32:10

1	particularly of this address translation logic	03:32:13
2	shown in Figure 7 in the grey box. A packet	03:32:18
3	would be generated, a TNet packet. There is some	03:32:20
4	hint as to how the TNet packet looks like. The	03:32:24
5	packet goes out, it percolates through the	03:32:27
6	system, the routing devices know how to do this.	03:32:30
7	At some point in time the packet is received by	03:32:33
8	the PCI interface and then, if it's done right,	03:32:35
9	one could implement something like that, and I	03:32:39
10	have done this in the PCI-SCI adapter, except	03:32:43
11	that the network is then SCI, that for a generic	03:32:47
12	write executed by the CPU, an ordinary memory	03:32:53
13	write of PCI would be executed. So one would	03:32:58
14	basically allow a certain sub-functionality of	03:33:02
15	PCI to be directly executed by the CPU for	03:33:05
16	performance reasons, at the end of the day mostly	03:33:08
17	will be probably reads and writes. All the other	03:33:10
18	functionality is a complex initialization,	03:33:14
19	configuration of these interfaces where the PCI	03:33:18
20	interface here is not detailed. That would be	03:33:23
21	part of the depacketizer functionality and	03:33:27
22	a configuration space which is not explicitly	03:33:35
23	shown. Every ASIC has a configuration space	03:33:37
24	having this complexity.	03:33:40
25	So it's far from being simple. And I	03:33:41

1	should also say I mean nothing of what I have	03:33:44
2	just said is disclosed in this reference, I just	03:33:46
3	responded like I would do something like that or	03:33:51
4	some high-level person and we are far away from	03:33:54
5	an ordinary-skill-in-the-art kind of person here,	03:33:57
6	we are requiring system-level understanding of	03:34:00
7	highly complex multi-parallel systems. We	03:34:02
8	require the understanding routing algorithms and	03:34:05
9	network deadlock resolution. These are all very	03:34:11
10	complex subjects which have to be taken into	03:34:14
11	account, otherwise the system will simply not	03:34:20
12	work.	03:34:23
13	Q. Let me unpack that a bit, that was	03:34:28
14	a lot.	03:34:32
15	So looking at Figure 2, one of the	03:34:33
16	things that is shown under the PCI interface is	03:34:38
17	a PCI controller.	03:34:42
18	A. Yes. Bottom right.	03:34:45
19	Q. Is that a standard PCI device?	03:34:48
20	MR. DAVIS: Objection; form.	03:34:50
21	THE WITNESS: Again, I mean, this is	03:34:55
22	a very high-level diagram, but it does say "PCI	03:34:56
23	controller". And applying the definition we have	03:35:01
24	been using, although I mean this is not a patent	03:35:06
25	here, I would assume that if somebody uses the	03:35:09

1	words "PCI" which are well defined in industry	03:35:14
2	then it's meant as a PCI as the PCI industry	03:35:17
3	standard, and by that argument chain it would	03:35:23
4	have to be a PCI-compliant device, correct.	03:35:26
5	BY MR. BUROKER:	03:35:26
6	Q. But does the term "controller"	03:35:30
7	suggest that it is something different than a PCI	03:35:32
8	device? Does the word "controller" mean anything	03:35:39
9	to you in this context?	03:35:43
10	A. I mean, we're here at	03:35:45
11	10,000 meters flight height, right, trying to see	03:35:50
12	little details. From this diagram I read we have	03:35:55
13	a PCI interface connected to the network, TNet,	03:35:59
14	and that means the primary path of communication	03:36:06
15	here is the PCI interface connected to TNet.	03:36:09
16	This is the particular ASIC we were discussing.	03:36:13
17	The PCI controller, why it's being	03:36:17
18	called "controller" I don't know and I don't want	03:36:21
19	to guess, but it is a device which is compliant	03:36:23
20	to PCI and this is even further emphasized by	03:36:25
21	showing that there is written "PCI" to this	03:36:30
22	single line interconnecting these two devices	03:36:34
23	which to me says this is a PCI bus, compliant PCI	03:36:37
24	bus.	03:36:42
25	Q. So the PCI controller, you're not	03:36:46

1	familiar strike that.	03:36:51
2	Is there a thing in the PCI nomenclature	03:36:53
3	of strike that.	03:37:01
4	Could this be a processor that operates	03:37:04
5	to control all of the other devices on the PCI	03:37:08
6	bus?	03:37:11
7	MR. DAVIS: Objection; form.	03:37:15
8	THE WITNESS: Other devices on this	03:37:22
9	particular local PCI bus as shown in Figure 2?	03:37:24
10	BY MR. BUROKER:	03:37:32
11	Q. Yes.	03:37:32
12	A. PCI is a bus which allows multiple	03:37:36
13	masters to operate, so from that point of view	03:37:40
14	this could be almost anything, including	03:37:47
15	a processor.	03:37:49
16	Q. And it would be possible that that	03:37:51
17	processor is the one that does at least the	03:37:54
18	initialization stage that you talked about for	03:38:00
19	the other PCI devices, that wakes them up and	03:38:02
20	gives them their addresses on that PCI bus?	03:38:06
21	MR. DAVIS: Objection; form.	03:38:11
22	THE WITNESS: This is highly	03:38:15
23	constructed and from the I mean, this diagram	03:38:18
24	is part of a paper written by a senior in the	03:38:26
25	field, Robert Horst, he is Technical Director at	03:38:30

1	Tandem Labs, so obviously he has reached a	03:38:37
2	relatively high level in his career and I would	03:38:40
3	consider him an expert.	03:38:44
4	What they invented and they have	03:38:49
5	quite a bit of discussion why they did that and	03:38:51
6	what it is for was to develop TNet to enable	03:38:53
7	a large number of computing devices, computer	03:38:57
8	processors and memory and this is also	03:39:04
9	indicated by the abstraction level here in	03:39:06
LO	Figure 2 where only CPU and memory is shown, not	03:39:08
11	even any TNet interface to enable them to	03:39:11
12	communicate very efficiently.	03:39:15
13	On top of that, of course such a large	03:39:17
L 4	system has to have an interface to the outside	03:39:19
L5	world, otherwise it wouldn't make any sense, and	03:39:22
L 6	for this reason all these additional devices, LAN	03:39:25
L7	controller, ATM controller, VME and PCI	03:39:34
L8	interfaces were created. To initialize such	03:39:37
L 9	a highly complex system through a remote PCI	03:39:42
20	interface to me would be taking the whole system	03:39:45
21	upside down. What you would do is you would	03:39:50
22	initialize the TNet system through the path for	03:39:52
23	which you built it and that is the processors	03:39:55
24	directly connected to it. There would have to be	03:39:58
25	a mechanism to identify which is the one selected	03:40:00

1	to perform the first initialization, a large	03:40:06
2	variety of different possible protocols possible,	03:40:11
3	nothing disclosed here. And then the	03:40:14
4	initialization would happen, and the PCI	03:40:17
5	interface would be much more complicated if it	03:40:19
6	would have to be built such that the	03:40:23
7	configuration and this initialization could be	03:40:25
8	done from the PCI side comfortably as well. I	03:40:27
9	wouldn't do that at all as an expert.	03:40:30
10	BY MR. BUROKER:	03:40:30
11	Q. So, the same example I asked you	03:40:34
12	about, if all of that were done, the	03:40:42
13	initialization and so forth, then the flow that	03:40:47
14	you describe just directionally would go from the	03:40:52
15	RISC CPU through the TNet processor interface	03:40:56
16	components?	03:41:01
17	A. Uh-huh.	03:41:03
18	Q. Next out onto the routers, one or	03:41:04
19	more routers, until it reached the PCI bus	03:41:07
20	interface that we've substituted for what's shown	03:41:12
21	in Figure 9.	03:41:14
22	A. Uh-huh.	03:41:15
23	Q. And then the PCI bus interface	03:41:16
24	would send it out on the PCI bus, something out	03:41:18
25	on the PCI bus which would be received by the	03:41:24

1	appropriate PCI device; is that right?	03:41:28
2	MR. DAVIS: Objection; form.	03:41:30
3	THE WITNESS: After the proper	03:41:31
4	initialization has been done, which I outlined,	03:41:34
5	correct.	03:41:36
6	BY MR. BUROKER:	03:41:37
7	Q. And what you've said in your	03:41:37
8	declaration was that until whatever information	03:41:38
9	this is got to the PCI interface, it would not be	03:41:41
10	a PCI bus transaction and the PCI bus transaction	03:41:46
11	would be created at this PCI interface; is that	03:41:50
12	correct?	03:41:53
13	A. That is correct, yes.	03:41:53
14	Q. Okay. So would you agree that in	03:41:55
15	that situation the information received by the	03:41:58
16	PCI interface would have to contain all of the	03:42:03
17	information needed to create a PCI bus	03:42:07
18	transaction?	03:42:13
19	MR. DAVIS: Objection; form.	03:42:14
20	BY MR. BUROKER:	03:42:18
21	Q. That information would need to be	03:42:18
22	there in order for to create a PCI bus	03:42:20
23	transaction, correct.	03:42:23
24	MR. DAVIS: Objection to form.	03:42:25
25	THE WITNESS: I mean I realize this is	03:42:29

1	a very complicated subject and the answer is not	03:42:30
2	easy. I believe I understand where you're trying	03:42:35
3	to get to but it's not that simple.	03:42:40
4	So, for example, we have to consider	03:42:43
5	where we start and where we end, right? We start	03:42:47
6	at the processor front side bus. And the	03:42:50
7	processor has a certain set of functionality it	03:42:54
8	can do. Most of that is cache coherency	03:42:59
9	functionality which we absolutely don't care in	03:43:02
10	the context of TNet even being put forward by	03:43:04
11	Horst saying, "We don't need cache coherency in	03:43:08
12	TNet" as opposed to SCI. There are 16 different	03:43:11
13	PCI transactions possible. So the only thing	03:43:15
14	that one can do or what people would try to do	03:43:21
15	which I did in the PCI-SCI adapter for some	03:43:24
16	performance, would be that if there is a certain	03:43:28
17	write transaction arriving, what you get is	03:43:31
18	an address, a virtual address in TNet land which	03:43:35
19	is recognized by the PCI interface, translated to	03:43:37
20	some other PCI address which has absolutely no	03:43:42
21	relation to the physical address used by the	03:43:47
22	processor at its front side bus, to then generate	03:43:51
23	a pre-configured PCI transaction for this address	03:43:56
24	range. So basically there is something	03:44:00
25	prearranged saying, "Well if I write to this	03:44:04

1	address please do a memory write" or, "Please do	03:44:06
2	a memory write multiple" or whatever other cycles	03:44:09
3	one would have and that would have to be	03:44:13
4	prearranged, could possibly even change over	03:44:16
5	time. That makes this game even more complicated	03:44:18
6	because usually it is very difficult to have	03:44:22
7	multiple independent processors doing the same	03:44:24
8	thing if you have a state, right? We call this	03:44:28
9	a state because it has a context. And I'm trying	03:44:30
10	to make it clear that you do not have, and you	03:44:34
11	cannot have in this context, the complete	03:44:36
12	information of the entire possible PCI context	03:44:40
13	here in the far end as part of the network	03:44:45
14	message going out.	03:44:49
15	BY MR. BUROKER:	03:44:49
16	Q. So, are you saying that it was not	03:44:51
17	possible to build a PCI bus transaction in that	03:44:54
18	it's just not possible to do because there's not	03:45:02
19	enough information coming in from the CPU?	03:45:04
20	A. No, no. As I said, you have	03:45:07
21	pre-configured interface here	03:45:10
22	Q. When you're saying "here" you're	03:45:13
23	referring to	03:45:15
24	A. Yes, you're right, pre-configured	03:45:15
25	interface, and I'm pointing to the right.	03:45:18

1	Q. The PCI interface box in Figure 2?	03:45:21
2	A. Correct.	03:45:25
3	Q. Go ahead.	03:45:27
4	A. Which instructs it to respond to	03:45:28
5	certain TNet commands in a certain way.	03:45:32
6	Q. Okay.	03:45:35
7	A. Right? And obviously the	03:45:36
8	instruction is, "Generate a particular PCI	03:45:40
9	transaction upon this TNet command". But there	03:45:43
10	is no PCI transaction then on TNet nor is there	03:45:46
11	the PCI address on TNet.	03:45:52
12	Let me try to make it even show you	03:45:57
13	the complexity at the example of a read	03:46:00
14	transaction because that makes a couple of things	03:46:07
15	even more obvious.	03:46:08
16	Q. Well, let me ask one question and	03:46:09
17	then I'll let you do that.	03:46:11
18	What you're saying is that the PCI	03:46:11
19	interface would take some information that it	03:46:13
20	received through this flow from the CPU plus	03:46:16
21	information it already had and then could compose	03:46:21
22	a PCI bus transaction?	03:46:25
23	A. That is correct.	03:46:27
24	Q. Okay. So some but not all of the	03:46:28
25	information needed to create a PCI bus	03:46:32

1	transaction would come through from the CPU down	03:46:34
2	through that flow to the PCI interface?	03:46:38
3	A. For the given transaction. It	03:46:41
4	would have to come through this flow via some	03:46:42
5	other commands beforehand, yeah.	03:46:45
6	Q. All right.	03:46:47
7	A. Because the only path is here.	03:46:48
8	Q. Right. So Figure 5 shows some	03:46:51
9	idea of the addressing format for a TNet	03:47:07
10	transaction; is that correct?	03:47:11
11	A. Yes.	03:47:14
12	Q. Okay. So I used the example of	03:47:15
13	a write request that would be from the CPU. So	03:47:18
14	according to this the write request would have	03:47:24
15	four sections: the header; the 4-byte TNet	03:47:26
16	address, which is referred to as the A; the D	03:47:31
17	box, which is zero to 64 bytes of data; and then	03:47:36
18	C which is the 4-byte CRC, which is basically	03:47:40
19	a hash, right?	03:47:45
20	A. It's an error correction.	03:47:47
21	Q. Error correction.	03:47:47
22	A. An error detection code, not	03:47:48
23	correction, sorry, CRC cannot correct errors.	03:47:51
24	Q. Error detection code, right. So	03:47:55
25	there are four pieces of information that would	03:47:57

1	be part of what the CPU in that situation would	03:47:58
2	send down the pipe heading for the PCI, assuming	03:48:00
3	everything has been initialized as you said,	03:48:07
4	right?	03:48:10
5	A. Uh-huh.	03:48:11
6	Q. Why would you need both	03:48:21
7	a destination ID, which is in the header, and	03:48:23
8	a four-byte TNet address? Wouldn't the 20-bit	03:48:29
9	destination ID be sufficient to identify where	03:48:33
10	you wanted the packets of data to go on the TNet	03:48:37
11	network?	03:48:42
12	MR. DAVIS: Objection; form.	03:48:43
13	THE WITNESS: The answer is no. This	03:48:49
14	is a bit a question of semantics and how Horst	03:48:55
15	chose to present this. And I mean this is a nice	03:49:00
16	question because it nicely shows the fundamental	03:49:05
17	difference between the two scenarios we have	03:49:07
18	here. Now, I go to Figure 2, which I don't like	03:49:10
19	because it's so abstract but now it helps. At	03:49:18
20	the top you see three boxes saying "CPU" and	03:49:22
21	"memory".	03:49:25
22	BY MR. BUROKER:	03:49:25
23	Q. Uh-huh.	03:49:26
24	A. And my leftover 16 gigabytes of	03:49:27
25	memory, at that time one didn't have that much,	03:49:35

1	but 32 bits of address space is not that much for	03:49:37
2	a CPU today. Even at that time computers were	03:49:41
3	starting to have hundreds of megabytes of main	03:49:44
4	memory. So the address space needed to simply	03:49:47
5	address the memory, let alone to address anything	03:49:50
6	outside that CPU, like the entire TNet world, is	03:49:53
7	the address space the local CPU has and this	03:49:58
8	other 32 bits, okay? And, for example, let's say	03:50:01
9	the left CPU is CPU 1, the middle is 2 and the	03:50:09
10	right one is 3. If CPU 1 wanted to read	03:50:14
11	an address from CPU 3 it would have to say which	03:50:17
12	address, and that would be an address of the	03:50:19
13	entire possible address space of CPU 3. So in	03:50:22
14	this context there would be 32 bits. Of course,	03:50:26
15	all modulo address translation, but at the final	03:50:29
16	end, when everything is said and done, that would	03:50:34
17	have to be the correct physical address of that	03:50:36
18	particular address in CPU 3.	03:50:38
19	The same game I can play for CPU 2. And	03:50:41
20	in parallel computing this is exactly what	03:50:45
21	happens, right? You have many, many computers	03:50:46
22	which compute a certain piece and then somebody	03:50:48
23	has to go gather everything. But you still have	03:50:50
24	to be able to identify which processor you want	03:50:53
25	the data from, and that's what is considered the	03:50:55

1	node address or node ID. And if you send	03:50:58
2	a packet, the packet is always sent from somebody	03:51:05
3	to somebody and, since you expect an answer, the	03:51:07
4	packet has to contain the sender ID, otherwise	03:51:10
5	the return wouldn't possibly work.	03:51:13
6	So in the TNet world, the source of	03:51:16
7	destination address is necessary to identify the	03:51:21
8	individual devices, the nodes, and the 4-byte	03:51:25
9	TNet address is basically the sometimes it's	03:51:33
10	called subaddress space identifying the devices	03:51:34
11	inside a node.	03:51:38
12	For example, in SCI case the semantic	03:51:39
13	was chosen slightly different, one has said SCI	03:51:43
14	has a 64-bit address space and the upper 16 bits	03:51:47
15	by definition are the node ID and the rest 48	03:51:48
16	bits are local addresses. Whether or not you	03:51:54
17	separate that out and give them different fields,	03:51:57
18	is really just a detail.	03:52:00
19	Q. Right, isn't it possible, it says	03:52:03
20	that on page 5, the TNet address is a 32-bit	03:52:05
21	window into the destination's address space,	03:52:11
22	right?	03:52:14
23	A. Yes.	03:52:14
24	Q. So for a PCI device, that would be	03:52:15
25	the 32-bit address of the PCI device?	03:52:18

1	A. Not necessarily.	03:52:20
2	MR. DAVIS: Objection to form.	03:52:22
3	BY MR. BUROKER:	03:52:24
4	Q. But it could be. So that you	03:52:24
5	could use the A field to fill in the PCI device	03:52:26
6	address and use the header information to tell	03:52:30
7	you where on the network that PCI device is	03:52:33
8	found?	03:52:37
9	MR. DAVIS: Objection; form.	03:52:38
10	THE WITNESS: What you're referring to	03:52:44
11	is one particular example of the address	03:52:46
12	translation on the receiving node would be simple	03:52:53
13	which doesn't mean the address translation on the	03:52:56
14	sending node is trivial as well, because hardly	03:52:59
15	ever the particular address you try to reach on	03:53:04
16	the PCI subsegment would be available like that	03:53:06
17	on the host node. It might be that there is just	03:53:14
18	local memory, right? And you have to also take	03:53:16
19	into account you have many possible devices which	03:53:24
20	you want to connect to. For every of those	03:53:32
21	devices you have to have an address window in the	03:53:35
22	physical address space of the host CPU 1, 2 or 3.	03:53:38
23	They can't be all at the same place, right? So	03:53:40
24	already there you see that the address windows	03:53:44
25	you have to have in the host CPU initiating the	03:53:47

1	transactions cannot map directly to the potential	03:53:52
2	address windows needed on the target device, the	03:53:57
3	PCI is only one example.	03:54:00
4	BY MR. BUROKER:	03:54:07
5	Q. What do you think that it means	03:54:07
6	when it says that the TNet address is a 32-bit	03:54:09
7	window into the destination's address space?	03:54:12
8	A. The destination address space	03:54:16
9	could be more than 32 bits.	03:54:17
10	Q. How do you get that from the word	03:54:25
11	"window", meaning that it's just a portion of	03:54:26
12	the	03:54:30
13	A. This is a term of art, being used	03:54:31
14	as that. So let's take this whole system as it	03:54:33
15	would be built today, then this CPU has a 64-bit	03:54:38
16	address space. And, let's say, I mean, the	03:54:44
17	computers we have recently built have 256	03:54:49
18	gigabytes of memory, so obviously there is no way	03:54:54
19	in this context with this TNet to address all 256	03:54:56
20	gigabytes. So in order for having	03:55:00
21	a communication, one would have to restrict	03:55:07
22	oneself to a 4-gigabyte sub-window in this huge	03:55:10
23	address space which could be exposed to other	03:55:14
24	nodes in TNet. But it may well be that every of	03:55:18
25	these CPUs gets a different window based on the	03:55:22

1	address translation table in the TNet interface.	03:55:27
2	Q. So then this document also talks	03:55:36
3	about something called an "address validation and	03:55:38
4	translation table".	03:55:40
5	A. Yes.	03:55:42
6	Q. And that's described as being the	03:55:43
7	thing that would map the CPU's physical address	03:55:44
8	space to the virtual TNet address space, right?	03:55:47
9	A. Uh-huh.	03:55:51
LO	Q. Okay.	03:55:52
L1	A. Figure 7. Now, this thing has to	03:55:54
L2	go both ways. And I mean, again, this is not	03:56:04
L3	disclosed in here, but this is something I'm sure	03:56:09
L 4	Horst knows and also so do I, if you build	03:56:15
L 5	a system of that scale, this is what's being	03:56:18
L 6	called a shared memory system, right, or	03:56:22
L7	a distributed memory system, allowing remote	03:56:27
L 8	direct access to the memory of other nodes inside	03:56:29
L 9	the system. When SCI was invented there was	03:56:33
20	a real war going on, very religious, as always,	03:56:38
21	between the distribute-shared-memory people and	03:56:43
22	the message-passing people. I mean these two	03:56:45
23	philosophies are maintained until today. So the	03:56:51
24	message-passing world says there is no	03:56:54
25	communication, direct communication to the local	03:56:58

1	memory of any other node, if you want to know	03:57:01
2	something you send a message saying, "Please tell	03:57:03
3	me what is stored there." And then the answer	03:57:05
4	comes back, usually requiring the processor to	03:57:07
5	actually actively respond. While the	03:57:09
6	shared-memory functionality says, "I grab	03:57:12
7	anything I just want." The caveat here is if you	03:57:14
8	have an error in any node, imagine you build	03:57:18
9	a system with a million processors I mean they	03:57:23
10	exist in the Blue Gene and one processor	03:57:26
11	starts writing funny nonsense to all sorts of	03:57:31
12	addresses on the remote nodes. Now you have	03:57:34
13	corrupted memory in another node and you have no	03:57:37
14	way of finding who caused it because no debugger	03:57:40
15	will possibly tell you that. That was the old	03:57:44
16	argument from the message-passing people against	03:57:46
17	the shared-memory people, saying, "You're	03:57:50
18	building a system which cannot be debugged." And	03:57:53
19	the shared-memory people said "Yeah, and your	03:57:55
20	message-passing interface is so slow we're ten	03:57:57
21	times faster." This is why there is more and	03:57:59
22	more, and this is here also indicated, access	03:58:03
23	protection built in, and this is why it's called	03:58:08
24	address validation, so access validation, so the	03:58:11
25	address translation tables in here basically	03:58:14

1	perform also the function of making sure that no	03:58:16
2	unauthorized access to any other addresses inside	03:58:19
3	the system is possible.	03:58:22
4	Q. So, let me just ask you some more	03:58:28
5	questions about this flow we've been talking	03:58:30
6	about. Is it your understanding that whatever	03:58:32
7	packet that would be created by the CPU and	03:58:38
8	passed through to the TNet processor interface,	03:58:41
9	that then that information is transmitted on the	03:58:47
10	physical layer, in other words over a cable, to	03:58:57
11	the next hop in the system which I guess would be	03:59:01
12	a router?	03:59:06
13	MR. DAVIS: Objection; form.	03:59:07
14	THE WITNESS: I have one problem with	03:59:12
15	your question because you said whatever packet	03:59:14
16	the CPU generated. The CPU does only memory	03:59:16
17	transactions, the packets happen in the TNet	03:59:21
18	processor interface. But aside from that	03:59:23
19	BY MR. BUROKER:	03:59:27
20	Q. So to be clear, some information	03:59:28
21	is sent from the CPU and at the TNet processor	03:59:31
22	a TNet packet is created and then it is placed on	03:59:36
23	the physical layer for transmission to the router	03:59:43
24	in Figure 9?	03:59:46
25	A. Yes.	03:59:47

1	Q. Okay.	03:59:48
2	A. And, I mean, one example of the	03:59:49
3	physical interface of TNet is Figure 4.	03:59:51
4	Q. Figure 4, right. And Figure 4	03:59:57
5	shows transmission over a cable that's used in	04:00:02
6	ECL?	04:00:10
7	A. Yeah.	04:00:11
8	Q. Right? ECL I guess it's called?	04:00:15
9	A. Yes.	04:00:17
10	Q. And do you agree with Mr. Young	04:00:21
11	that that is a form of low-voltage differential	04:00:24
12	signalling? Not the industry standard LVDS but	04:00:28
13	a form of low-voltage differential signalling?	04:00:33
14	A. The inventors of LVDS would now	04:00:43
15	yell and scream because LVDS was invented to do	04:00:45
16	away with ECL. ECL was the way signals were	04:00:52
17	communicated it's a differential standard, too	04:01:00
18	if things had to be fast. But ECL has been	04:01:03
19	extremely power hungry and usually is defined on	04:01:07
20	negative voltages which is the last thing you	04:01:12
21	really want in low-voltage ASICs these days.	04:01:16
22	It's a current signal, as it says,	04:01:20
23	emitter-coupled logic. The emitter drains	04:01:24
24	basically the current onto the cable. Voltages	04:01:27
25	only happen based on the termination scheme. I'm	04:01:29

1	not sure whether or not ECL is really	04:01:36
2	an established standard such as the IEEE 1596.3.	04:01:39
3	At 50,000 meters flight height one might say	04:01:48
4	there is certain similarities, but low-voltage	04:01:52
5	differential signalling, in particular the	04:01:56
6	original LVDS standard, was created to avoid ECL.	04:01:58
7	So I would not consider this in the broader	04:02:04
8	context. Now, if you say this is a differential	04:02:08
9	signal that is certainly correct.	04:02:13
10	Q. Right, and it is differential	04:02:16
11	signalling you agree with that?	04:02:20
12	A. Absolutely, yes.	04:02:21
13	Q. Okay. The question is whether	04:02:22
14	it's low voltage or not I guess is the issue,	04:02:26
15	right?	04:02:29
16	A. Yeah.	04:02:32
17	Q. And you say LVDS was a well-known	04:02:39
18	improvement over ECL for low-voltage differential	04:02:44
19	signalling?	04:02:48
20	A. LVDS is a big improvement over	04:02:49
21	ECL. As you can see ECL doesn't exist anymore.	04:02:53
22	I mean these computers all use LVDS, for	04:02:55
23	instance, to talk to the graphics display which	04:02:58
24	is by far the fastest, probably the fastest	04:03:00
25	connection inside laptop computers. I was	04:03:05

1	pointing to a laptop computer. ECL, for it being	04:03:09
2	so very power hungry and for all the other	04:03:14
3	disadvantages I just quoted, is, in this context,	04:03:17
4	not being used.	04:03:20
5	Q. This figure shows the information	04:03:26
6	the TNet packet going through an 8B/9B encoder.	04:03:31
7	A. Yeah.	04:03:38
8	Q. Do you agree that that is a form	04:03:39
9	of encoding that meets the claim strike	04:03:41
10	that that meets the term in the claim 24 of	04:03:46
11	the '814 Patent?	04:03:49
12	A. It is one form of encoding and it	04:03:55
13	does fit the definition of encoding which I set	04:03:57
14	forth but it is not the particular incarnation of	04:04:00
15	encoding which has been used in this patent.	04:04:03
16	Q. Right, but if something uses is	04:04:05
17	it 8-bit/9-bit or 8-byte/9-byte?	04:04:09
18	A. Bit, 8-bit/9-bit encoder.	04:04:12
19	Q. Normally capital B mean byte.	04:04:13
20	It's confusing.	04:04:17
21	So if somebody is using 8-bit/9-bit	04:04:18
22	encoding then that would be the kind of encoding	04:04:22
23	that is contemplated in claim 24 of the '814	04:04:26
24	Patent, right?	04:04:31
25	A. If you would have said this is	04:04:41

1	a kind of encoding according to the definition I	04:04:43
2	set forth, yes.	04:04:45
3	Q. Okay.	04:04:46
4	A. Now, I mean, to be honest, I mean,	04:04:47
5	since I'm under oath and I'm trying to be really	04:04:51
6	as accurate as I can possibly be, my	04:04:54
7	understanding is these terms, as they are	04:04:56
8	construed in the patent, have to be seen in the	04:04:58
9	light of the patent document. This patent	04:05:01
10	document doesn't discuss 8B/10B encoding or 8B/9B	04:05:05
11	encoding or $4B/5B$ encoding, these are the typical	04:05:11
12	standards. In fact 8B/9B is not very common.	04:05:16
13	And since you specifically asked for claim 24	04:05:19
14	this is now a detail of patent law I'm not 100	04:05:23
15	percent sure how to answer.	04:05:27
16	Q. Okay. You agree though that	04:05:29
17	what's shown in Figure 4 is a serial transmission	04:05:43
18	of data between what says "Cabinet B" and	04:05:47
19	"Cabinet A"?	04:05:51
20	MR. DAVIS: Objection to form.	04:05:52
21	THE WITNESS: If we go to the	04:05:56
22	definition I put forth for what is serial and	04:05:58
23	we looked at that already so I don't want to	04:06:01
24	repeat it but it basically says if a certain	04:06:03
25	amount of information is transmitted over	04:06:07

1	a smaller number of signals, then taking into	04:06:09
2	account that processors at the time where this	04:06:13
3	was published at the time when the patents were	04:06:17
4	filed were typically 32 bits or more, then it	04:06:21
5	is consistent to be a serial transmission, right?	04:06:27
6	8 bits aren't much less than 32.	04:06:33
7	BY MR. BUROKER:	04:07:05
8	Q. So let me ask you then, the flow	04:07:05
9	of data we've been talking about, looking at	04:07:17
10	Figure 8, the TNet packet would come in and be	04:07:27
11	received at the TNet interface and be stored in	04:07:35
12	a packet buffer's just something to store	04:07:39
13	things while other packets are being processed;	04:07:42
14	is that right?	04:07:45
15	MR. DAVIS: Objection; form.	04:07:46
16	THE WITNESS: What really happens	04:07:53
17	inside these packet buffers depends on a lot of	04:07:54
18	things which are not disclosed in here. So, for	04:07:57
19	example, if TNet would I don't remember the	04:08:01
20	clock rate, whether there are any clock rates	04:08:09
21	specified here, what is the transmission speed of	04:08:11
22	TNet but if TNet would be much faster than the	04:08:13
23	particular bus interface here, such as PCI, then	04:08:18
24	it could happen that this interface cannot work	04:08:21
25	off the packets at the speeds being arrived.	04:08:25

1	Then there is typically what one	04:08:28
2	implements, so-called derandomizing buffers, to	04:08:32
3	basically absorb a burst of writes. Of course	04:08:36
4	that can only be done to a certain extent and in	04:08:40
5	fact the size of such buffers has been always	04:08:43
6	a long debate where lots of simulations are being	04:08:46
7	done to find an optimum, because if you put in	04:08:49
8	too much it just costs money and it's never being	04:08:51
9	used and if you put in too little you introduce	04:08:54
10	a lot of flow control on the network saying,	04:08:56
11	"Wait, wait, wait, can't do any more,	04:08:59
12	slowing things down" and so forth.	04:09:01
13	The second reason for the packet	04:09:03
14	buffers is once the packet is being received,	04:09:06
15	there needs to be a decoding done, it needs to be	04:09:08
16	understood what particular transaction should	04:09:11
17	result from that, then the interface, once it	04:09:13
18	recognized okay, "I need to do this transaction",	04:09:16
19	it needs to acquire the PCI bus, so there has to	04:09:19
20	go out a PCI bus request, a bus arbiter has to	04:09:23
21	say, "You can" or, "You have to wait". When it	04:09:26
22	says, "Bus granted, you can use the bus", it	04:09:28
23	still has to wait for any possibly still ongoing	04:09:30
24	bus transaction to finish. So these are random	04:09:33
25	times causing delays, random delays. And only	04:09:36

1	after all of that has happened then the PCI	04:09:39
2	transaction can happen, and then only the data	04:09:42
3	which is starting to be accumulated here can be	04:09:45
4	drained.	04:09:50
5	So a rule of thumb is the minimum size	04:09:51
6	of such a packet buffer would be the maximum	04:09:55
7	packet size which could be received because	04:09:57
8	otherwise you would risk losing data coming in	04:10:01
9	and the buffer being full.	04:10:04
10	BY MR. BUROKER:	04:10:04
11	Q. So out of the buffer would be some	04:10:08
12	information that would be depacketized. At what	04:10:12
13	point in this were you contemplating that the PCI	04:10:15
14	bus transaction would be generated?	04:10:19
15	A. I mean that would have to happen	04:10:26
16	in the bus interface, or I would put it into the	04:10:28
17	context of the bus interface.	04:10:32
18	Q. Yeah, but of these boxes in the	04:10:34
19	bus interface, where would that take place? Oh,	04:10:35
20	the one that just says "bus interface"? The long	04:10:39
21	box that says "bus interface"	04:10:42
22	A. Exactly.	04:10:45
23	Q within the square that says	04:10:46
24	"TNet bus interface"?	04:10:47
25	A. I mean, yeah. What you have here	04:10:48

1	is, again, there's just so many details which are	04:10:52
2	implicit here but not obvious and not really	04:11:01
3	shown. But if you look at the TNet link, this	04:11:03
4	has got to be something running at relatively	04:11:07
5	high clock rates. You have PCI on the other	04:11:10
6	side, comparably slow clock rates. What comes in	04:11:14
7	is byte write, right? I mean 9 bits but it's	04:11:20
8	basically bytes in one or the other form, as	04:11:26
9	outlined in the document here basically where	04:11:30
10	is it? Yes, in fact, it's not explicitly in here	04:11:41
11	at all. But obviously it can't be more than 9	04:11:52
12	bits. In fact, no, it can only be 8 bits because	04:11:54
13	it's an 8B/9B encoder and PCI is at least	04:11:58
14	32 bits, so this whole thing has to be expanded,	04:12:02
15	which is the functionality of the depacketizer.	04:12:06
16	So you have a TNet interface with a rather high	04:12:10
17	clock rate going into the packet buffers, and	04:12:13
18	then the context depacketizer suggests that here	04:12:15
19	the unframing is done, the word width is	04:12:20
20	recreated. The packetizer would probably try to	04:12:23
21	extract already the addresses and separate them	04:12:28
22	from the data, create nice 32-bit data word	04:12:33
23	chunks and so forth, and then the bus interface	04:12:37
24	would have to know what to do with this kind of	04:12:40
25	thing. And again Figure 8, of course, has to	04:12:42

1	have all the functionality in there that is also	04:12:46
2	shown in Figure 7. So we, again, have address	04:12:48
3	validation, translation, access control, the	04:12:51
4	whole nine yards, which is not shown here at all.	04:12:56
5	This is not something I would put as	04:12:59
6	sub-functionality of the bus interface. In fact,	04:13:03
7	I don't know where I would put this. I would say	04:13:06
8	this is just missing here as abstracted away now.	04:13:07
9	Q. But under that scenario, if a PCI	04:13:15
10	bus transaction was created, it would be then	04:13:18
11	sent on the PCI bus to be received by the PCI	04:13:25
12	device to which it was addressed, right?	04:13:33
13	A. Correct.	04:13:36
14	MR. DAVIS: Objection to form.	04:13:37
15	BY MR. BUROKER:	04:13:38
16	Q. For that PCI device to act on the	04:13:38
17	transaction, whatever the transaction is?	04:13:41
18	A. (The witness nodded.)	04:13:43
19	Q. Right? So, would you agree at	04:13:45
20	a minimum that in that scenario the CPU has	04:13:49
21	transmitted information that was used to create	04:13:55
22	a PCI bus transaction?	04:14:01
23	MR. DAVIS: Objection; form.	04:14:04
24	THE WITNESS: Could you define	04:14:07
25	"information that was used" a little bit more	04:14:15

1	specific?	04:14:17
2	BY MR. BUROKER:	04:14:17
3	Q. I'm trying to use in its broadest	04:14:18
4	sense, not trying to call it data, not trying to	04:14:21
5	call it address bits, just saying if the CPU sent	04:14:23
6	information that was received by and interpreted	04:14:26
7	by a PCI bus device?	04:14:36
8	MR. DAVIS: Objection; form.	04:14:39
9	THE WITNESS: The problem why I'm	04:14:43
10	hesitant to answer is there is some information	04:14:45
11	sent by the CPU which finally results in the PCI	04:14:49
12	transaction which, however, requires additional	04:14:53
13	other information which has to be set up earlier	04:14:55
14	in the context of everything, thereby the	04:14:58
15	information all by itself is not sufficient to	04:15:01
16	create such a PCI transaction. Therefore I'm not	04:15:04
17	sure whether I should say yes.	04:15:07
18	BY MR. BUROKER:	04:15:12
19	Q. And one of the reasons why you say	04:15:12
20	that Horst doesn't disclose everything in, for	04:15:13
21	example, claims 24 and 31, is that there is no	04:15:18
22	northbridge or peripheral bridge to communicate	04:15:23
23	all of the pieces of information of a PCI bus	04:15:28
24	transaction in serial form, right?	04:15:31
25	MR. DAVIS: Objection; form.	04:15:35

1	BY MR. BUROKER:	04:15:36
2	Q. That's one of the opinions you	04:15:37
3	offer. Like the header on page 85 of your '814	04:15:40
4	declaration.	04:15:47
5	MR. DAVIS: Objection; form.	04:15:56
6	THE WITNESS: I mean I do stand by what	04:15:58
7	I wrote in my report.	04:15:59
8	BY MR. BUROKER:	04:16:01
9	Q. And that's because no matter what	04:16:02
10	it's your view that what's transmitted over the	04:16:07
11	TNet network are TNet packets. That's the second	04:16:10
12	sentence of paragraph 129, right?	04:16:13
13	A. Yeah.	04:16:18
14	Q. And it's your view that the TNet	04:16:19
15	packets don't have all of the information to	04:16:23
16	compose a PCI transaction and, therefore, the	04:16:27
17	entire PCI bus transaction is not sent as part of	04:16:34
18	the TNet packet, right?	04:16:36
19	MR. DAVIS: Objection; form.	04:16:37
20	THE WITNESS: I mean in Horst, because	04:16:46
21	you say the entire PCI transaction is not sent	04:16:47
22	over the TNet, that would suggest that there is	04:16:50
23	a PCI bus here having PCI transactions. There is	04:16:52
24	no PCI transaction anywhere in this whole	04:16:57
25	architecture except for the far end inside the	04:17:00

1	controller. And I'm really happy to discuss this	04:17:03
2	further but could have a short break now?	04:17:06
3	MR. BUROKER: Sure, we'll go off the	04:17:11
4	record.	04:17:13
5	(Brief recess taken 4:17 p.m 4:27 p.m.)	04:17:13
6	BY MR. BUROKER:	04:27:10
7	Q. So let's talk about that same	04:27:14
8	configuration we've been talking about, but where	04:27:20
9	the PCI device wants to communicate with the CPU	04:27:22
10	and, you know, all the caveats you had earlier	04:27:31
11	about how it had to be configured and all that	04:27:35
12	sort of stuff. But in that case the PCI device	04:27:38
13	would originate a PCI transaction up the PCI bus,	04:27:41
14	right?	04:27:45
15	A. Of course, there is no other way.	04:27:46
16	Q. And that would then get routed to	04:27:51
17	the PCI bus interface that's shown in Figure 2	04:27:54
18	and that we, you know, assume looks something	04:28:06
19	like what's in Figure 8, right?	04:28:08
20	A. Yes, but before we go further	04:28:14
21	Q. Oh, I'm sorry, that's not right.	04:28:16
22	So the PCI device would communicate and that	04:28:18
23	would go to the PCI bus interface which would	04:28:20
24	connect to a TNet bus interface or would it be	04:28:25
25	a TNet PCI bus interface? I'm confused.	04:28:31

1	MR. DAVIS: Objection; form.	04:28:36
2	THE WITNESS: Yeah, I mean, according	04:28:37
3	what we discussed earlier I would say, if we look	04:28:39
4	at Figure 8, this is the PCI bus and that would	04:28:42
5	interface through this interface to TNet as	04:28:47
6	a system with everything. And what happens at	04:28:50
7	the far end then depends what target node is	04:28:53
8	being addressed. But before we go into details	04:28:56
9	I would like to know are we talking now read	04:28:59
10	transaction, write transaction, what transaction?	04:29:03
11	BY MR. BUROKER:	04:29:06
12	Q. I think I said, but let me	04:29:06
13	clarify, a write transaction. So the PCI wants	04:29:07
14	to write something into the memory associated	04:29:09
15	with one of the remote CPUs shown in Figure 9.	04:29:12
16	A. Uh-huh.	04:29:25
17	Q. Right? So it would start with	04:29:26
18	a PCI bus transaction of a write command type, it	04:29:28
19	would be transmitted on the PCI bus, right?	04:29:33
20	A. Yeah.	04:29:37
21	Q. That would end up at the PCI bus	04:29:38
22	interface which would then create a TNet packet,	04:29:42
23	correct?	04:29:48
24	A. No.	04:29:49
25	Q. What's wrong with what I said?	04:29:51

1	A. It would create one or multiple	04:29:53
2	TNet packets because PCI bus transactions can	04:29:56
3	have a certain length and they can certainly have	04:29:59
4	more than 64 bytes being transmitted, that really	04:30:02
5	depends on what device you have. So, for	04:30:06
6	example, in here you have disks connected, there	04:30:09
7	could be a PCI rate controller having a disk and	04:30:14
8	disk blocks are 512 bytes. But TNet, referring	04:30:17
9	to Figure 5, allows only zero to 64 bytes of	04:30:22
10	data. That means if there is a longer ongoing	04:30:28
11	PCI transaction that would result in multiple	04:30:32
12	TNet packets being generated, whatever size	04:30:34
13	packets then will depend on the detailed	04:30:39
14	configuration, but there is no one-to-one	04:30:42
15	relationship between a TNet packet and a bus	04:30:44
16	transaction, on either side be it a processor or	04:30:46
17	be it PCI.	04:30:49
18	Q. Right, but the data would be the	04:30:50
19	same. The data of a PCI bus transaction that is	04:30:51
20	of a write command would go directly into the	04:30:56
21	data field of a TNet packet, correct?	04:31:01
22	MR. DAVIS: Objection to form.	04:31:07
23	THE WITNESS: It would be at the	04:31:10
24	THE COURT REPORTER: I didn't get the	04:31:16
25	last word of the answer sorry, you were all three	04:31:16

1	speaking at the one time. You said, "It would be	04:31:16
2	at the"?	04:31:19
3	BY MR. BUROKER:	04:31:19
4	Q. I'll just start over.	04:31:19
5	So the data of a PCI transaction of	04:31:20
6	a write command variety, would then be filled in	04:31:23
7	to the data portion of a TNet packet, correct?	04:31:25
8	MR. DAVIS: Objection; form.	04:31:33
9	THE WITNESS: The data would go through	04:31:36
10	the 8B/10B encoder as shown in Figure 4, but you	04:31:41
11	can also nicely see the decoder to it to complete	04:31:47
12	the symmetry. And on TNet there would be	04:31:50
13	an encoded version of it. The data would be	04:31:52
14	physically different but it could be recreated	04:31:56
15	then by the 9B/8B decoder.	04:31:59
16	BY MR. BUROKER:	04:32:03
17	Q. And let's just say my write	04:32:04
18	transaction I'm talking about a small amount of	04:32:06
19	data, less than 64 bytes, then there would be one	04:32:08
20	TNet packet that would need to be encoded to be	04:32:13
21	transmitted over the TNet links, right?	04:32:19
22	MR. DAVIS: Objection to form.	04:32:20
23	THE WITNESS: I assume so. This is one	04:32:28
24	way it could be done, yeah. The reason why I'm	04:32:34
25	a bit careful here is the following. There are	04:32:38

1	often alignment requirements on data as to be put	04:32:44
2	into packets. That means if you have a 32-byte	04:32:48
3	write you want to do but it starts off at an odd	04:32:57
4	address starting at address offset, say, 47,	04:33:02
5	which means the 32 bytes align 32-byte blocks.	04:33:05
6	It often happens that two network packets are	04:33:10
7	being created for efficiency reasons. This	04:33:12
8	really depends on lots of details how these	04:33:16
9	interfaces are implemented. There is no clear	04:33:21
10	indication in this document how it is being done,	04:33:26
11	but this is something which happens a lot.	04:33:29
12	BY MR. BUROKER:	04:33:29
13	Q. A simple form would be to take	04:33:31
14	just the data out of the PCI bus transaction and	04:33:33
15	fill it into the data component of the TNet	04:33:37
16	transaction and if there's any leftover space	04:33:43
17	just pad it with zeros, right? That's one way to	04:33:46
18	do it?	04:33:49
19	MR. DAVIS: Objection; form.	04:33:50
20	THE WITNESS: You can't pad with zeros,	04:33:54
21	because it would mean you write more data	04:33:57
22	which	04:33:59
23	BY MR. BUROKER:	04:33:59
24	Q. Well, it's	04:34:00
25	A. And you don't have to, because the	04:34:01

1	TNet packet has a length word which allows it to	04:34:07
2	be of variable length. But the padding is being	04:34:11
3	done in case of other networks which have	04:34:15
4	fixed-length packets where basically zeros are	04:34:17
5	being padded but then there is still an indicator	04:34:21
6	which of the bytes are actually valid.	04:34:25
7	Q. Forget what I said. A simple form	04:34:29
8	of transmission of the data would be to just take	04:34:32
9	the data from the PCI bus transaction, fill it	04:34:35
10	into the data field and then set the data link to	04:34:38
11	indicate the exact length of that data from the	04:34:45
12	bus transaction?	04:34:48
13	MR. DAVIS: Objection to form.	04:34:49
14	THE WITNESS: And this is one possible	04:34:50
15	way it can be done, yet it's not disclosed here	04:34:56
16	in particular.	04:34:59
17	BY MR. BUROKER:	04:35:02
18	Q. And what is why your view about	04:35:05
19	what would happen to the other pieces of the PCI	04:35:07
20	bus transaction as part of the process to create	04:35:10
21	the TNet packet?	04:35:19
22	MR. DAVIS: Objection; form.	04:35:22
23	THE WITNESS: What do you mean with the	04:35:23
24	other portions?	04:35:24
25	BY MR. BUROKER:	04:35:27

1	Q. So the address, the command, the	04:35:27
2	control line and the byte enables, the other	04:35:29
3	things. You know there's 47 bits that we talked	04:35:32
4	about on the PCI bus transaction, what happens to	04:35:36
5	the rest of those bits of data?	04:35:38
6	MR. DAVIS: Objection; form.	04:35:42
7	THE WITNESS: I would expect the TNet	04:35:47
8	interface not to respond to all or not to	04:35:50
9	transform all the particular PCI commands into	04:35:56
10	TNet functionalities. So, for example, I	04:36:01
11	wouldn't say any way to, for instance, do a PCI	04:36:06
12	configuration cycle for TNet, right?	04:36:10
13	What we are doing here is we're jumping	04:36:14
14	forth and back between a higher abstraction layer	04:36:16
15	and more transaction and physical layer inside	04:36:21
16	these buses and that can cause confusion,	04:36:24
17	therefore I would like to be really careful.	04:36:26
18	There is the class of read	04:36:30
19	transactions, there is the class of write	04:36:32
20	transactions and there is a whole subclass of	04:36:34
21	read transactions which is in PCI defined as	04:36:36
22	a read configuration, read I/O, read memory. In	04:36:39
23	case of a processor you have yet another set of	04:36:46
24	kinds of reads, the entire span of cache	04:36:50
25	coherency protocols which are all flavors of	04:36:56

1	reads. TNet just can do a read, nothing else.	04:36:58
2	So all the other functionality behind is gone	04:37:05
3	inside TNet and has to be, if needed, recreated	04:37:11
4	by some auxiliary infrastructure we already	04:37:14
5	discussed.	04:37:18
6	So, in this case, I would expect the	04:37:19
7	interface between PCI and TNet to be configured	04:37:22
8	after everything is initialized to basically	04:37:25
9	respond to memory reads and memory writes. That	04:37:28
10	would be the easiest thing, and that would be the	04:37:31
11	context in which I expect this document to be	04:37:35
12	written namely having an I/O device, being PCI,	04:37:39
13	which has produced some data, which it wants to	04:37:46
14	deliver to some CPU, and in this context we don't	04:37:49
15	need to understand the difference between a read,	04:37:53
16	a read multiple, or a write line or whatever, we	04:37:55
17	don't need to understand cache coherency, we just	04:37:57
18	need that data to find its way all the way	04:38:00
19	through the system to the far end, to the memory,	04:38:02
20	right? But there is no one-to-one correlation	04:38:05
21	between any given PCI transaction and any given	04:38:11
22	TNet packet.	04:38:13
23	And, I mean, I understand this is it	04:38:17
24	important and I think it becomes really, really	04:38:18
25	clear if you take a read transaction, because	04:38:23

1	writes can be posted, reads cannot.	04:38:27
2	BY MR. BUROKER:	04:38:27
3	Q. But to continue what we were	04:38:31
4	talking about, a write PCI bus transaction is	04:38:33
5	sent and the TNet interface, the TNet-PCI	04:38:43
6	interface creates one or more TNet packet that	04:38:49
7	gets sent over the same set of components, the	04:38:54
8	routers and so forth, and they end up at the	04:38:59
9	processor interface associated with the correct	04:39:03
10	CPU, correct?	04:39:08
11	A. Provided all the translation	04:39:09
12	tables, everything is initialized properly, yeah.	04:39:11
13	Q. Okay. And so then that processor	04:39:14
14	interface, the TNet processor interface, would	04:39:17
15	then pass the TNet packet, it would create	04:39:20
16	whatever form of bus transaction the CPU was	04:39:31
17	expecting, right?	04:39:34
18	MR. DAVIS: Objection to form.	04:39:37
19	BY MR. BUROKER:	04:39:40
20	Q. Looking at Figure 7 in that	04:39:40
21	line between the TNet processor facing the RISC	04:39:42
22	CPU, for example, there would be some interface	04:39:47
23	that would create perhaps a CPU bus transaction,	04:39:50
24	right?	04:39:54
25	A. This figure, to me, isn't	04:39:56

1	perfectly clear. If I take this figure and one	04:39:59
2	has to be really careful with these very high	04:40:04
3	level figures, but if I take this figure and take	04:40:07
4	it literally, we could say if there is a write	04:40:09
5	transaction arriving at the TNet link there is	04:40:12
6	absolutely no need to bother the CPU on the	04:40:15
7	system bus, because that ASIC here sorry, this	04:40:19
8	TNet processor interface, which I assume to be	04:40:22
9	an ASIC because it has to be quite fast, has	04:40:24
10	a direct memory interface, even part of this	04:40:26
11	design block, so it could perform the write	04:40:30
12	transaction directly to the memory without	04:40:32
13	bothering the CPU. So, in an extreme case, there	04:40:35
14	could be a write transaction coming in, being	04:40:39
15	executed against the memory by the CPU, execute	04:40:41
16	another transaction against TNet to some other	04:40:43
17	address sending a network packet out, because	04:40:46
18	network is able to submit and receive	04:40:50
19	simultaneously.	04:40:52
20	However and this is the reason why	04:40:53
21	I'm puzzled, this is bad style because that	04:40:55
22	means the snooping functionality of that RISC	04:40:58
23	CPU	04:40:58
24	Q. The what kind of functionality?	04:41:05
25	A. Snooping, like Snoopy.	04:41:07

1	Q. Okay, that's what I thought you	04:41:08
2	said but I wanted to make sure.	04:41:09
3	A. This is a term of art, believe it	04:41:11
4	or not, and it really comes from Snoopy being	04:41:13
5	very nosy.	04:41:16
6	Q. So the snooping functionality.	04:41:24
7	A. It means the following. These	04:41:27
8	CPUs, and I've shown you all of them have caches,	04:41:30
9	and if you have data in a cache and somebody else	04:41:33
10	writes to memory, it can happen that the data	04:41:40
11	written to is the data of which you have a cached	04:41:44
12	copy. Yeah?	04:41:48
13	Q. Right.	04:41:50
14	A. If that happens, aside from the	04:41:50
15	CPU without the CPU knowing, you have what we	04:41:53
16	call a stale copy. And if you have a system	04:41:55
17	which allows you to have a stale copy of a cache,	04:42:00
18	you have created a computer which is not working,	04:42:02
19	or you have to do a whole lot in software on top	04:42:08
20	of that. The only remedy to this problem would	04:42:12
21	be that every time you try to read something from	04:42:15
22	an area where you suspect somebody could have	04:42:18
23	possibly written, meaning you have an enabled	04:42:22
24	remote access to that region, you have to flush	04:42:24
25	the caches. Now, flushing caches is something	04:42:27

1	extremely expensive you really don't want to do.	04:42:30
2	So this is why processors have a functionality,	04:42:33
3	they basically watch what is happening on the	04:42:36
4	bus. Like somebody else comes in, writes to the	04:42:38
5	memory, the processor says, "Wait a minute I want	04:42:41
6	to see what you're doing here." Then it compares	04:42:43
7	the physical addresses on that bus, and if then	04:42:45
8	there is a match to a cache line being hit,	04:42:47
9	either the cache line is being invalided as safe	04:42:50
10	or, even fancier, the processor sorry the	04:42:54
11	cache does that, looks what is the data being	04:42:59
12	transmitted and copies it simultaneously while it	04:43:01
13	goes from memory into the cache line and then you	04:43:03
14	still have a coherent cache line, yeah? And	04:43:05
15	caches were well known at that time and were very	04:43:13
16	important already. So this figure here certainly	04:43:16
17	leaves something out or doesn't mention something	04:43:18
18	which would be quite useful to have.	04:43:20
19	Q. Well at a minimum the CPU would be	04:43:22
20	connected to the main memory through something	04:43:24
21	other than the TNet processor interface, right?	04:43:27
22	MR. DAVIS: Objection; form.	04:43:30
23	THE WITNESS: I mean the way it's drawn	04:43:32
24	here has some deficiencies.	04:43:34
25	BY MR. BUROKER:	

1	Q. But in like Figure 2 it shows them	
2	like connected	
3	A. Yeah, but this is so abstract in a	
4	way	
5	Q or drawn together, right?	
6	A. But in Figure 2 the memory talks	04:43:46
7	directly to the TNet and this is obviously not	04:43:48
8	happening.	04:43:51
9	Q. Okay, so in that situation,	04:44:00
10	somehow or another the TNet processor link has	04:44:04
11	taken the packet created a transaction to write	04:44:09
12	the data that came from our PCI bus device into	04:44:15
13	memory.	04:44:21
14	A. Uh-huh.	04:44:22
15	Q. Right?	04:44:23
16	MR. DAVIS: Objection; form.	04:44:23
17	BY MR. BUROKER:	04:44:27
18	Q. So is it fair to say that the CPU	04:44:28
19	main memory components received PCI bus	04:44:33
20	transaction information or not?	04:44:40
21	MR. DAVIS: Objection; form.	04:44:42
22	THE WITNESS: They received the payload	04:44:43
23	of a PCI write, they did not receive a PCI	04:44:47
24	transaction, it's not there anymore, it's	04:44:54
25	something else.	04:44:59

1	BY MR. BUROKER:	04:44:59
2	Q. And when would you say the PCI bus	04:45:00
3	transaction in that flow ceased to exist?	04:45:03
4	A. Exactly at the moment where it	04:45:08
5	leaves the PCI to TNet interface. In the very	04:45:10
6	moment where the packetizing starts to happen, we	04:45:15
7	have something else. For it to continue to exist	04:45:18
8	one would have to be able to show that all the	04:45:24
9	states and functionality defined in here would	04:45:27
10	have to still be present.	04:45:30
11	Q. And that's based on your	04:45:32
12	understanding of the TNet strike that of	04:45:33
13	the term "PCI bus transaction". Would you agree	04:45:35
14	if a broader interpretation of PCI bus	04:45:40
15	transaction was adopted by the PTAB here, which	04:45:43
16	just required some of the information from a PCI	04:45:51
17	bus transaction, that in that definition the CPU	04:45:53
18	memory elements have received at least a portion	04:46:02
19	of the PCI bus transaction, the payload?	04:46:04
20	MR. DAVIS: Objection; form.	04:46:07
21	THE WITNESS: I'm not aware of such a	04:46:09
22	definition.	04:46:10
23	BY MR. BUROKER:	04:46:12
24	Q. I'm just saying and this is	04:46:12
25	a hypothetical if they were to adopt it, would	04:46:14

1	you agree that at least you said the payload	04:46:19
2	would be received; is that correct?	04:46:20
3	MR. DAVIS: Objection; form.	04:46:22
4	THE WITNESS: These what-if discussions	04:46:26
5	are dangerous because they are highly	04:46:29
6	hypothetical. In that case I would like to	04:46:31
7	review the exact wording of the adopted	04:46:33
8	definition, then I would like to take my time and	04:46:35
9	really verify this against the patent claims and	04:46:39
10	the entire prior art cited in order to give	04:46:42
11	a competent answer. But upon some very generic I	04:46:46
12	think this is quite difficult. And, second,	04:46:49
13	I would have a problem because you cannot talk	04:46:52
14	about a standard and then say we just take part	04:46:54
15	of it because then it's not a standard anymore.	04:46:56
16	I mean, this is the fundamental principle of the	04:46:58
17	definition of such a thing. You have to have the	04:47:05
18	complete functionality or it won't work.	04:47:08
19	BY MR. BUROKER:	04:47:08
20	Q. Right, well, but claim 24 never	04:47:14
21	identifies a PCI device that has to use that	04:47:19
22	information, right?	04:47:23
23	MR. DAVIS: Objection to form.	04:47:27
24	THE WITNESS: There is no PCI device	04:47:41
25	explicitly mentioned in claim 24, yet	04:47:43

1	BY MR. BUROKER:	04:47:45
2	Q. Of the '814 Patent?	04:47:46
3	A. Of the 814 Patent, correct.	04:47:48
4	Q. Right.	04:47:50
5	A. Yet a PCI transaction is executed	04:47:50
6	in order to communicate with the PCI device,	04:47:54
7	nothing else makes any sense. So this is	04:47:57
8	implicitly clearly stated here. It's implicitly	04:47:59
9	included so I should say.	04:48:05
10	Q. But it's not explicitly included?	04:48:05
11	A. Sorry, I misspoke. I am sorry,	04:48:12
12	it's implicitly included.	04:48:14
13	Q. But based on what? Just because	04:48:16
14	it uses the word "PCI bus transaction" you're	04:48:18
15	saying implicitly it requires that there be a PCI	04:48:22
16	bus device to be able to receive and process it?	04:48:26
17	MR. DAVIS: Objection; form.	04:48:27
18	THE WITNESS: For what other reason	04:48:29
19	would you execute a PCI transaction?	04:48:30
20	BY MR. BUROKER:	04:48:31
21	Q. Well, it doesn't say you execute	04:48:31
22	a PCI transaction.	04:48:33
23	MR. DAVIS: Objection; form.	04:48:34
24	BY MR. BUROKER:	04:48:36
25	Q. Does it?	04:48:36

1	A. " the north bridge to	04:48:43
2	communicate address and data bits of a PCI	04:48:43
3	transaction in serial form"	04:48:50
4	going on further and further. What	04:48:50
5	would the purpose be to communicate a PCI	04:48:52
6	transaction somewhere unless one wanted to	04:48:58
7	execute such PCI transaction?	04:49:00
8	Q. I don't know. It's one of the	04:49:01
9	the claim doesn't say that you have to execute	04:49:03
10	a PCI bus transaction, correct?	04:49:05
11	MR. DAVIS: Objection; form.	04:49:10
12	BY MR. BUROKER:	04:49:12
13	Q. Claim 24 of the '814 Patent.	04:49:12
14	A. Well, if you read the patent it's	04:49:15
15	quite obvious it's stated in here.	04:49:17
16	Q. Right, but your job and the PTAB's	04:49:20
17	job is to compare what's in the claim to the	04:49:23
18	prior art. So claim 24 doesn't explicitly say	04:49:27
19	that a PCI bus transaction has to be executed,	04:49:29
20	correct?	04:49:33
21	MR. DAVIS: Objection; form.	04:49:36
22	THE WITNESS: I mean I believe I	04:49:47
23	already answered. I believe it is implicitly	04:49:48
24	included, but it's not explicitly stated, yes.	04:49:50
25	BY MR. BUROKER:	04:49:50

1	Q. So is that part of the	04:49:56
2	interpretation of claim 24 that you used in	04:49:57
3	looking at the prior art? You were looking to	04:49:58
4	make sure that the prior art actually executed	04:50:00
5	PCI bus transactions that are communicated from	04:50:03
6	the northbridge?	04:50:07
7	MR. DAVIS: Objection; form.	04:50:09
8	THE WITNESS: No, I mean I have	04:50:13
9	outlined how I looked at these claims, and the	04:50:15
10	discussion we conduct is whether or not there is	04:50:18
11	an encoded I mean one of the areas we're	04:50:22
12	discussing here, aside from the other	04:50:25
13	functionality such as address translation and	04:50:28
14	coding, were whether or not there were encoded	04:50:32
15	PCI transactions on the discussed network, which	04:50:34
16	are in the two references SCI and TNet.	04:50:37
17	BY MR. BUROKER:	04:50:37
18	Q. Right. And then is your opinion	04:50:43
19	also the same that having a PCI bus transaction	04:50:45
20	that can be executed is implicitly required by	04:50:51
21	claim 31 of the '814 Patent and claim 54 of the	04:50:54
22	'873 Patent?	04:51:03
23	MR. DAVIS: Objection; form.	04:51:06
24	THE WITNESS: I mean in the context of	04:51:20
25	PCI transaction it clearly says:	04:51:21

1	" a peripheral bridge coupled to	04:51:23
2	said microprocessor unit without any intervening	04:51:25
3	Peripheral Component Interconnect (PCI) bus, said	04:51:27
4	peripheral bridge coupled to second LVDS channel	04:51:31
5	to communicate address and data bits of PCI bus	04:51:34
6	transaction in serial form over said second	04:51:34
7	channel."	04:51:34
8	And this is what I used to evaluate.	04:51:38
9	BY MR. BUROKER:	04:51:44
10	Q. But if the peripheral bridge in	04:51:45
11	chamber 31 transmits the PCI bus transaction that	04:51:50
12	never gets received and never gets executed as	04:51:55
13	a result, is it your understanding that the claim	04:51:59
14	has been met or not met?	04:52:02
15	A. It strict sense it has been met,	04:52:05
16	but it wouldn't make any sense to build a system	04:52:07
17	like that. And you would be hard pressed to find	04:52:09
18	one.	04:52:13
19	Q. Well, you'd find one where the PCI	04:52:15
20	device was broken and didn't receive the	04:52:17
21	transaction, it would still have been sent,	04:52:21
22	right?	04:52:23
23	MR. DAVIS: Objection; form.	04:52:25
24	BY MR. BUROKER:	04:52:28
25	Q. So there are circumstances in	04:52:28

1	which a device may send a PCI bus transaction to	04:52:29
2	a device and nothing happens because that device	04:52:32
3	is broken.	04:52:35
4	A. Yeah, but this would be a highly	04:52:40
5	constructed special case and the system was still	04:52:43
6	built to communicate between this host and the	04:52:46
7	PCI device and, in such an exceptional case,	04:52:49
8	a transaction would fail but it would still be	04:52:54
9	legitimate transaction on the bus, it would time	04:52:56
10	out, and be responded to as an error.	04:52:58
11	Q. So is it fair to say that one of	04:53:05
12	the reasons why you believe that the term "PCI	04:53:07
13	bus transaction" requires the entirety of the PCI	04:53:10
14	specification is because otherwise execution of	04:53:15
15	the claim doesn't make any sense?	04:53:24
16	MR. DAVIS: Objection; form.	04:53:26
17	THE WITNESS: The claim says "PCI bus	04:53:31
18	transaction", PCI is a well-defined standard, so	04:53:33
19	this is basically just already stated right here.	04:53:35
20	That it wouldn't make any sense above and beyond	04:53:39
21	is a different story, but I believe it is	04:53:42
22	sufficient that it says here "PCI bus	04:53:43
23	transaction" and, I mean, we have discussed	04:53:46
24	before that under the broadest reasonable	04:53:48
25	interpretation, this is how it would have to be	04:53:50

1	interpreted.	04:53:54
2	BY MR. BUROKER:	04:53:54
3	Q. In your view for the Horst	04:54:03
4	reference, would any of the address information	04:54:04
5	in that PCI bus transaction that was originated	04:54:09
6	by our PCI device be conveyed to the memory CPU?	04:54:13
7	A. You mean that some bits of the	04:54:20
8	original PCI transaction ended up being the same	04:54:22
9	at the far end? Is that the message? I'm not	04:54:26
10	sure I understand.	04:54:29
11	Q. Right, yeah.	04:54:30
12	A. Well, you have to	04:54:31
13	Q. Not randomly the same. Let me ask	04:54:33
14	it differently.	04:54:36
15	So the scenario we talked about where	04:54:39
16	you've got a PCI bus transaction that's started	04:54:41
17	by a PCI device and sent up through the pipe	04:54:42
18	towards the CPU and memory, that scenario.	04:54:45
19	A. Uh-huh.	04:54:48
20	Q. Would any of the information from	04:54:49
21	the PCI bus transaction that was created, the	04:54:51
22	address information, find its way up through the	04:54:56
23	TNet system to the CPU/memory?	04:55:00
24	MR. DAVIS: Objection; form.	04:55:04
25	THE WITNESS: To answer that question	04:55:08

1	I would have to have a definition of the address	04:55:09
2	translation in this document and I'm pointing	04:55:13
3	to the Horst reference is actually being done,	04:55:15
4	this is not disclosed at all. There is no	04:55:18
5	indication, as far as I know, unless you point me	04:55:21
6	to it and I overlooked it, which says how it	04:55:25
7	works in particular. It is typically done as	04:55:29
8	a table lookup, but typically done doesn't mean	04:55:32
9	it is done like this here or it is obviously to	04:55:35
10	do it like that.	04:55:37
11	BY MR. BUROKER:	04:55:41
12	Q. And what do you mean by "a table	04:55:41
13	lookup", what would that mean? Would the address	04:55:43
14	information in the PCI bus transaction be	04:55:45
15	included in the TNet	04:55:51
16	A. No.	04:55:53
17	Q packet?	04:55:55
18	A. As far as I know, there is no	04:56:01
19	address translation which is done or even	04:56:06
20	possible which is functioning through some sort	04:56:09
21	of an algorithm, right, you calculate the	04:56:12
22	translated address. There is many reasons for	04:56:18
23	it. It is always done like that. You have	04:56:21
24	a particular address which you like to translate	04:56:25
25	and then there is a bunch of tables which can	04:56:28

1	have a rather complex form, they can be	04:56:30
2	hierarchical, where the translated address is	04:56:36
3	being searched. Now, what is the granularity of	04:56:40
4	those tables or how the particular searching	04:56:43
5	algorithm works depends on the particular	04:56:46
6	implementation and there is nothing disclosed in	04:56:51
7	Horst, and I therefore don't wish to speculate,	04:56:53
8	but in my declaration I put an example of	04:56:56
9	an address translation which is in the book by	04:56:59
10	Dave Patterson and Hennessy, right? There is	04:57:04
11	a diagram which shows one way it's being done as	04:57:09
12	an example.	04:57:12
13	Q. Do you know where that is in your	04:57:13
14	declaration?	04:57:15
15	A. I'm already looking. I got the	04:57:16
16	wrong here, here is '873. Page 20, for example.	04:57:18
17	Q. Which declaration?	04:57:41
18	A. '814.	04:57:42
19	Q. Okay.	04:57:52
20	A. Before we go into details, one	04:57:53
21	again has to be very clear that an address is	04:57:56
22	only valid if you have all bits. Like	04:57:58
23	a telephone number, if I take off two or three	04:58:00
24	bits of telephone number, the rest of the bits	04:58:03
25	have no meaning, or you need to dial a lot of	04:58:04

1	numbers before you reach the right number.	04:58:08
2	The way it is usually being done in	04:58:12
3	computers, sorry, in processors so you are far	04:58:14
4	outside the TNet context now but in case of	04:58:20
5	a microprocessor there are the address	04:58:23
6	translation where the main memory is broken up	04:58:29
7	into so-called pages. The size of a page is	04:58:32
8	a fixed thing and depends really on the	04:58:35
9	architecture of the processor, and that has some	04:58:38
10	reasons which are quite complicated and have to	04:58:41
11	do with the fact that one tries to make the	04:58:46
12	address translation as efficient as possible,	04:58:48
13	allowing it to happen in parallel to the cache	04:58:50
14	lookup. Typical page sizes are 4 kilobytes. And	04:58:54
15	that means for every virtual address, the upper	04:58:59
16	bits beyond the 4 kilobytes are basically that	04:59:02
17	page number being addressed, right? You could	04:59:08
18	say page number 0, 1, 2, 3, 4, 5 until you	04:59:12
19	reached the full space. This is what he calls	04:59:15
20	the virtual page number. That goes into	04:59:19
21	a translation scheme. Extremely oversimplifying	04:59:21
22	you could say this is a table which basically has	04:59:20
23	as index this virtual page number and as content	04:59:31
24	the physical page number to which it translates	04:59:35
25	to. In reality it's not done like that, that	04:59:38

1	simple, because then these tables would become	04:59:42
2	huge, consuming	04:59:45
3	Q. You're looking at page	04:59:50
4	A. Page 20.	04:59:52
5	Q. Page 20 of the '814?	04:59:53
6	A. '814. Ah wait yeah '814.	04:59:55
7	There you are but how come it's on the left page	05:00:14
8	in your case?	05:00:15
9	Q. This is the '873 declaration.	05:00:17
10	A. Oh, I can also use the '873	05:00:21
11	declaration, it doesn't matter. Just let me find	05:00:24
12	it here.	05:00:27
13	Q. Oh, I know why, I'm looking at	05:00:30
14	page 20 of the response, it's my fault. It's	05:00:32
15	been a long day.	05:00:36
16	Page 20, we're on the same page, 20 of	05:00:37
17	the '814. Okay, I see where you're talking	05:00:41
18	about.	05:00:44
19	A. So typically this translation	05:00:45
20	scheme are multiple references to main memory of	05:00:46
21	the computer trying to find the right page	05:00:50
22	number, but for the simplicity of the argument	05:00:54
23	you could consider this as a one-step process	05:00:58
24	being a large, large single vector. That means	05:01:00
25	the physical address is assembled by the	05:01:04

1	translated physical page number and the lower 12	05:01:09
2	address bits which are the same as the virtual	05:01:14
3	address. This is how a microprocessor does it.	05:01:17
4	This is how basically every processor does it	05:01:20
5	with implementation variance on the translation	05:01:23
6	table itself. And for every process in the	05:01:27
7	system you have an individual private address	05:01:29
8	translation table, meaning for every virtual	05:01:32
9	address scope you have such a table.	05:01:37
10	Q. Okay, but going back in	05:01:41
11	paragraph 135 of the '814 declaration, you say	05:01:42
12	because:	05:01:48
13	" TNet address are virtual addresses	05:01:48
14	that TNet address cannot be PCI standard	05:01:52
15	addresses which are physical addresses."	05:01:57
16	A. Yeah.	05:01:59
17	Q. But couldn't you just fill in the	05:02:04
18	PCI bus address field into the A field of your	05:02:13
19	TNet packet?	05:02:17
20	MR. DAVIS: Objection	05:02:20
21	BY MR. BUROKER:	05:02:21
22	Q. 32 bits for 32 bits, you couldn't	05:02:22
23	do that?	05:02:24
24	MR. DAVIS: Objection; form.	05:02:24
25	THE WITNESS: What would it help you?	05:02:26

1	I mean I tried to outline that in a TNet system	05:02:31
2	like that, you have so many different address	05:02:38
3	spaces and every node has its own predefined	05:02:41
4	local physical address space already, right? So,	05:02:45
5	you can't just use any arbitrary PCI address to	05:02:51
6	address something inside this target node because	05:02:57
7	they wouldn't match. That doesn't rule out that	05:03:02
8	under some extreme rare conditions in one	05:03:06
9	particular case there would be a trivial	05:03:10
10	translation, but the general case is certainly	05:03:13
11	not correct.	05:03:15
12	BY MR. BUROKER:	05:03:16
13	Q. Well what about in a situation	05:03:17
14	where instead of having multiple CPU memories,	05:03:18
15	like you see in Figure 9, you just had one? So	05:03:22
16	all of the devices on the PCI bus could use an	05:03:33
17	addressing scheme that would map to the memory,	05:03:43
18	the single CPU memory?	05:03:48
19	MR. DAVIS: Objection; form.	05:03:50
20	BY MR. BUROKER:	05:03:54
21	Q. So that you could then use the PCI	05:03:54
22	bus address straight into the TNet address field?	05:03:56
23	MR. DAVIS: Objection; form.	05:04:03
24	BY MR. BUROKER:	05:04:05
25	Q. Is that possible is my question.	05:04:05

1	MR. DAVIS: Objection; form.	05:04:07
2	THE WITNESS: I mean you're trying to	05:04:11
3	re-engineer TNet back to a PCI hierarchical	05:04:14
4	single-node system. I would have to consider	05:04:19
5	that. It's not disclosed at all or even	05:04:24
6	suggested in this disclosure here. It wouldn't	05:04:27
7	make much sense to use the system as such.	05:04:31
8	BY MR. BUROKER:	05:04:39
9	Q. But your testimony is that what	05:04:39
10	would make sense would be to throw away the	05:04:41
11	address piece of a PCI bus transaction and create	05:04:44
12	a new one. Is that right?	05:04:48
13	A. To map	05:04:50
14	MR. DAVIS: Objection; form.	05:04:50
15	THE WITNESS: you have to lay out	05:04:52
16	an address scheme for all of the devices	05:04:55
17	involved. In order to implement that you have	05:04:58
18	your address translation. Whether or not in	05:05:00
19	a particular case the translation could be	05:05:08
20	trivial, I don't know it's possible, but it's	05:05:11
21	certainly not the general case and it's certainly	05:05:19
22	not indicated in here, and it would make it	05:05:21
23	unlikely that this system works with a large	05:05:29
24	number of nodes. And still you wouldn't have	05:05:32
25	a PCI transaction in the far end because then	05:05:39

1	there is just an ordinary CPU.	05:05:41
2	BY MR. BUROKER:	05:05:51
3	Q. Right, but in that scenario, if	05:05:52
4	you took the address information and the data	05:05:53
5	information out of the PCI bus transaction and	05:05:58
6	you communicated both of those through TNet	05:06:00
7	packets up to the CPU/memory, you would have	05:06:03
8	communicated at least the address and data	05:06:09
9	information of a PCI bus transaction to	05:06:13
10	a northbridge, right?	05:06:16
11	MR. DAVIS: Objection; form.	05:06:17
12	THE WITNESS: In order to know whether	05:06:28
13	or not that could possibly work we would have to	05:06:30
14	really study the details of a particular	05:06:32
15	processor, the already predefined address maps	05:06:35
16	inside that system, same for the PCI subsystem.	05:06:39
17	And if that all would work out and one could	05:06:45
18	create such an address map, which would be more	05:06:48
19	like a lucky windfall and only work for a rather	05:06:51
20	like you constructed a single-node system in	05:06:56
21	my mind then you would transmit the	05:06:59
22	information of the PCI transaction. You would	05:07:05
23	still not transmit the PCI transaction, the	05:07:08
24	payload.	05:07:11
25	BY MR. BUROKER:	05:07:14

1		Q.	Did you know Dr. Horst?	05:07:14
2		Α.	No.	05:07:16
3		Q.	Have you ever seen this TNet	05:07:17
4	article c	n the	IEEE?	05:07:21
5		Α.	I did not.	05:07:23
6		Q.	Did you receive IEEE publications?	05:07:25
7		Α.	We have them in the library, in	05:07:33
8	fact I ha	ve pu	rchased them, grinding my teeth	05:07:38
9	because i	t's r	eally expensive. But there is	05:07:41
10	a lot of	mater	ial. I certainly didn't read all	05:07:45
11	IEEE pape	ers, t	here's no way I could do that.	05:07:48
12		Q.	Sure. And had you ever heard of	05:07:51
13	the TNet	syste	m?	05:07:52
14		Α.	No.	05:07:53
15		Q.	And you knew who Tandy Tandy or	05:07:54
16	Tandem?			05:07:57
17		Α.	Tandem.	05:07:57
18		Q.	Tandem Computer Company was,	05:07:59
19	right?			05:08:01
20		Α.	(The witness nodded.)	05:08:01
21		Q.	Had you ever done any work with	05:08:02
22	Tandem Co	mpute	r Company before well, had you	05:08:04
23	ever done	work	with Tandem Computer Labs?	05:08:06
24		Α.	Not that I'm aware of. In fact, I	05:08:10
25	mean for	me TN	et would have not been something	05:08:15

1	highly exciting because the reasoning for	05:08:19
2	developing it is not something I follow to	05:08:26
3	100 percent because, for example, they argue that	05:08:36
4	SCI is useless to them because of all the added	05:08:38
5	complexity of the cache coherency protocols,	05:08:42
6	neglecting the detail that there is	05:08:45
7	a non-coherent version of SCI which is exactly	05:08:47
8	what I have been using, so to me there would have	05:08:51
9	been no benefit switching technologies. Then	05:08:53
10	TNet would have been something proprietary by	05:08:55
11	Tandem. Highly unclear whether or not these	05:08:58
12	network devices would be sold openly on the	05:09:03
13	market, which is a strict requirement for us	05:09:06
14	being able to use this technology. It would be	05:09:10
15	a sole source. Sole sources are a big problem if	05:09:12
16	you build these large-scale systems with a plan	05:09:16
17	15 or 20 years in the future. This is why we	05:09:21
18	really like standards in this context, therefore,	05:09:24
19	that was likely for me not to show up on my radar	05:09:28
20	screen. And if somebody in my contacts would	05:09:31
21	have seen it, it would most likely not have been	05:09:34
22	something where somebody would have said, "Hey,	05:09:39
23	you really have to read this."	05:09:41
24	MR. BUROKER: I'm about to move to	05:09:49
25	a different subject, why don't we take a break	05:09:50

1	and go off the record.	05:09:50
2		05:09:50
3	(Volume I of II in the deposition of Volker	05:09:52
4	Lindenstruth concluded at 5:09 p.m.)	
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1	ACKNOWLEDGEMENT OF DEPONENT
2	I, VOLKER LINDENSTRUTH, do hereby certify that I
3	have read the foregoing transcript of my testimony taken
4	on $8/27/15$, and further certify that it is a true and
5	accurate record of my testimony (with the exception of
6	the correction listed below):
7	Page Line Correction
8	II
9	
10	
11	
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20	
21	
22	VOLKER LINDENSTRUTH
23	SUBSCRIBED AND SWORN TO BEFORE ME
24	THIS, 20
25	

2	UNITED KINGDOM:
3	I, Audrey Shirley, accredited court
4	reporter, do herby certify that the witness whose
5	deposition is hereinbefore set forth appeared
6	before me in London, United Kingdom on the 27th
7	day of August 2015, at 8:57 a.m.; was duly sworn
8	before the commencement of the deposition; that
9	the testimony was taken down by me using machine
10	shorthand; that all appearances of counsel and
11	participants hereto are noted on the appearance
12	page; and that such deposition is a true,
13	correct, and full record of the proceedings.
14	I further certify that I am not related
15	to nor employed by any of the parties to this
16	action; that I am not employed by counsel for any
17	of the parties to this action; and that I am in
18	no way interested in the outcome of this matter.
19	IN WITNESS WHEREOF, I have hereunto set
20	my hand this 27th day of August 2015.
21	
22	
23	Anorey Shurley
24	1100109
25	AUDREY SHIRLEY, Court Reporter

REPORTER'S CERTIFICATION

1

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